

for VE

Ramos-15L

CPU : Ivy Bridge BGA
Chip Set : Intel Panther Point
GFX : NV N14M_GL/N14P_GV2
INTEL HD 3000/4000
Remarks : Chief River Platform

Model Name : Ramos-15L
PBA Name : MAIN
PCB Code : BA41-02317A (GCE/HST/PTC)

Dev. Step : PV
Revision : 1.0
T.R. Date : 2013.06.01

Design	CHECK	APPROVAL
Pei Wang	RJ Zheng	BL LEE

Owner : SEC Mobile R & D Signature : X

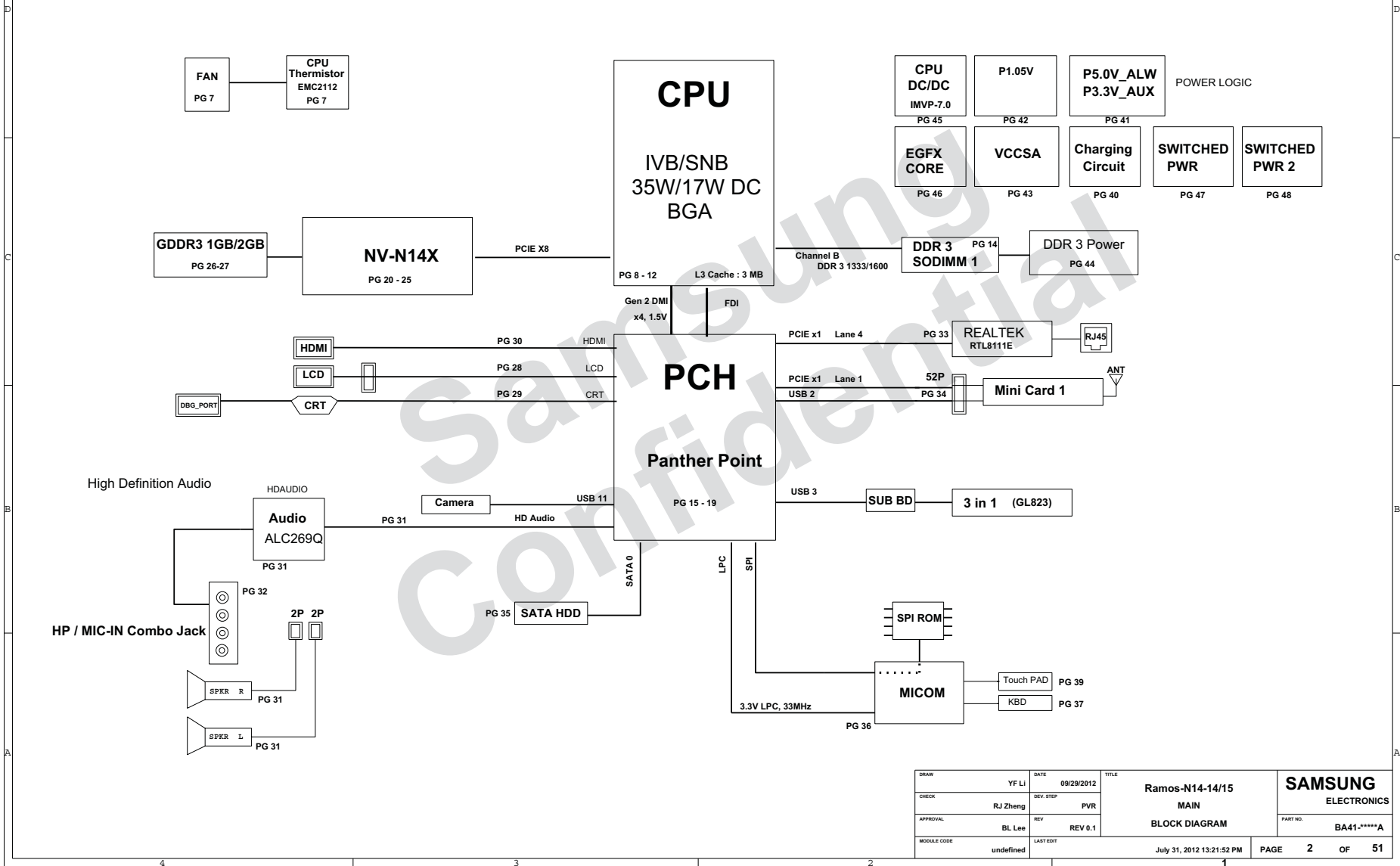
sheet01 : Cover
sheet02 : BLOCK DIAGRAM
sheet03 : BOARD INFORMATION
sheet04 : POWER DIAGRAM
sheet05 : CLOCK DISTRIBUTION
sheet06 : Green Clock
sheet07 : Thermal Sensor
sheet08 : CPU-IvyBridge (1/5)
sheet09 : CPU-IvyBridge (2/5)
sheet10 : CPU-IvyBridge (3/5)
sheet11 : CPU-IvyBridge (4/5)
sheet12 : CPU-IvyBridge (5/5)
sheet13 :
sheet14 : DDR3 SODIMM1
sheet15 : PCH-PantherPoint (1/5)
sheet16 : PCH-PantherPoint (2/5)
sheet17 : PCH-PantherPoint (3/5)
sheet18 : PCH-PantherPoint (4/5)
sheet19 : PCH-PantherPoint (5/5)
sheet20 : NV-N14X (1/5)
sheet21 : NV-N14X (2/5)
sheet22 : NV-N14X (3/5)
sheet23 : NV-N14X (4/5)
sheet24 : NV-N14X (5/5)
sheet25 : NV-N14X STRAP
sheet26 : GFX memory
sheet27 : GFX memory
sheet28 : LVDS / CAMERA
sheet29 : VGA
sheet30 : HDMI
sheet31 : Audio - ALC269Q-VC-GR
sheet32 : Audio - Combo Jack
sheet33 : LAN (Realtek RTL8111E)
sheet34 : WLAN
sheet35 : SATA interface (HDD I/F)

sheet36 : MICOM / BIOS(MEC1310)
sheet37 : MICOM Glue Logic
sheet38 : USB3.0 connector
sheet39 : MAIN TO SUB CONNECTOR
sheet40 : Power - charger
sheet41 : Power - P3.3V_AUX / P5.0V_AUX
sheet42 : Power - P1.05V (Chipset Power)
sheet43 : Power - VCCSA
sheet44 : Power - DDR3
sheet45 : Power - CPU VRM
sheet46 : Power - EGFX_CORE
sheet47 : Power - Switched Power 1
sheet48 : Power - Switched Power 2
sheet49 : Power - Power Discharge
sheet50 : Mount Hole
sheet51 : SUB (TOUCHPAD)

DRAW	LI, YF	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS
CHECK	ZHENG, RJ	REV. STEP	PVR	MAIN		
APPROVAL	LEE, BL	REV	REV 0.1	COVER		
MOBILE CODE		LAST EDIT			PART NO. BA41-*****A	
				December, 17, 2012 1:42:04 PM	PAGE 1 OF 51	

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BLOCK DIAGRAM



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails		Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail	S4 - S5
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR3 (off in S4-S5)	S3
P6.0V P3.3V P1.8V P1.5V P0.75V P0.85V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.75V power rail for DDR3 (off in S3-S5) 0.85V switched power rail (off in S3-S5)	S0
VCC_CORE EGFX_CORE P1.05V (VCCP)	Core Voltage for CPU Core Voltage for GPU VCC for PANTHERPOINT	S0

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	1	NC
2	Multi Memory Card Controller	2	NC
3	SYSTEM PORT 2	3	LAN CONTROLLER
4	NC	4	NC
5	NC	5	NC
6	NC	6	NC
7	NC	7	NC
8	HSDPA		
9	NC		
10	Mini PCI Express (WLAN)		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	NC
2	NC
3	NC
4	NC
5	NC

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	PANTHER POINT	Real Time Clock
Crystal	25MHz	Green Clock	REALTEK
Crystal	27MHz	N14M	

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

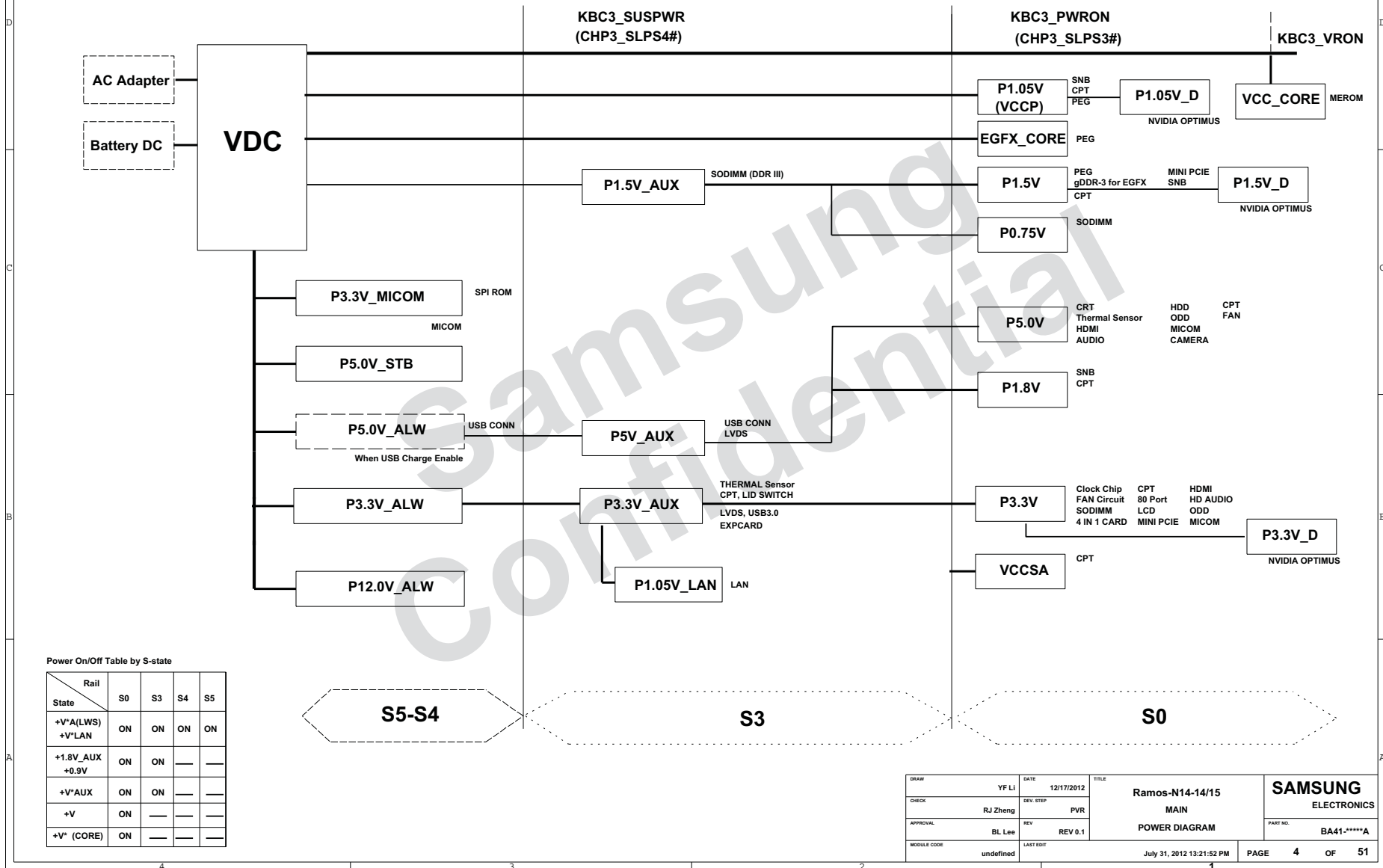
I ² C / SMB Address			
Devices	Address	Hex	Bus
PANTHERPOINT	Master	-	SMBUS Master
CPU Thermal Sensor	0011 000X	30h	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
on board DDR3 thermal Sensor	1001 100x	98h	-
Platform thermal management TS	1001 011x	96h	-

DRAW	YF Li	DATE	12/17/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	RJ Zheng	DEV. STEP	PVR		MAIN	
APPROVAL	BL Lee	REV	REV 0.1		BOARD INFO	
MODULE CODE	undefined	LAST EDIT		July 31, 2012 13:21:52 PM	PAGE 3 OF 51	

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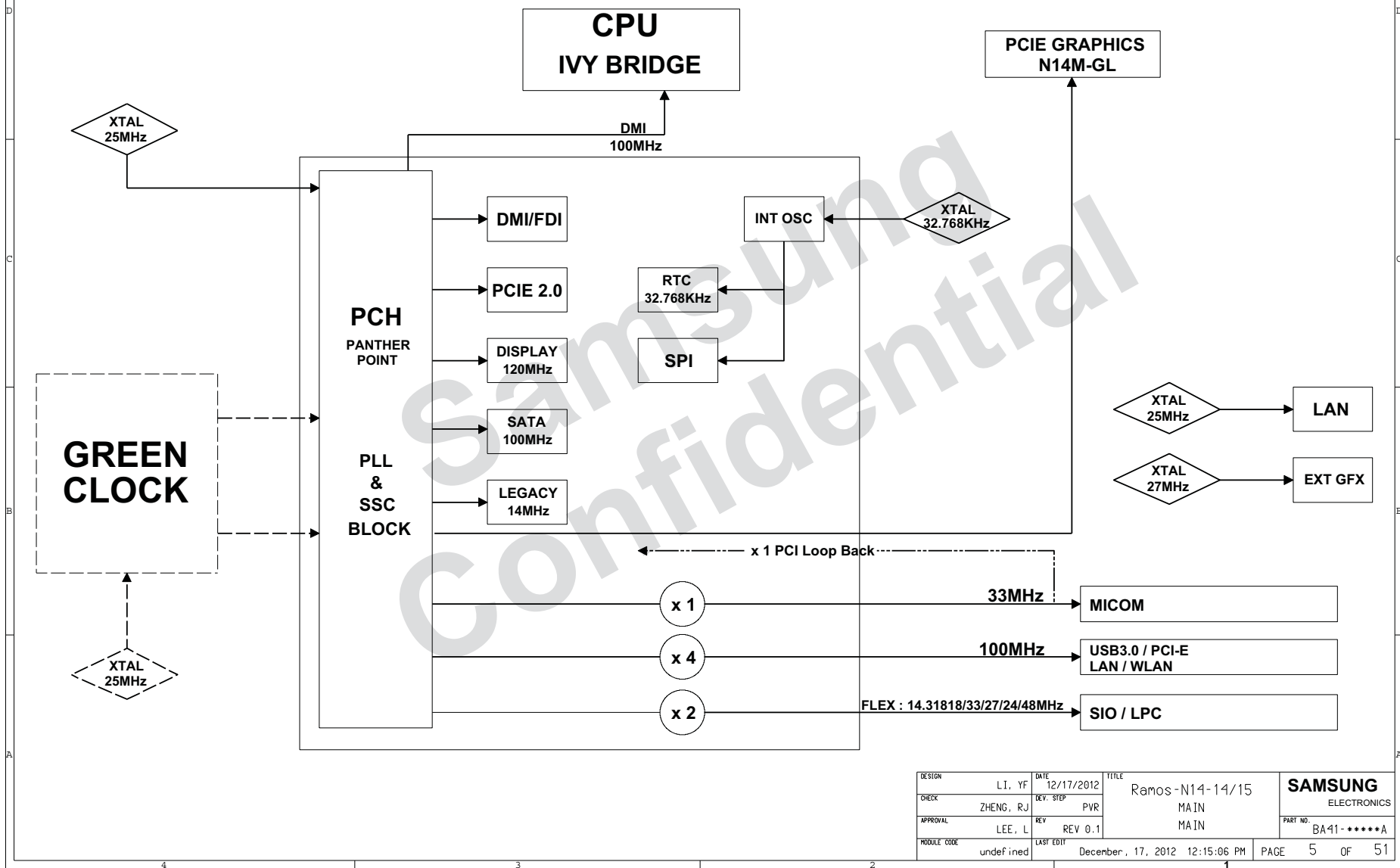
POWER DIAGRAM

Rev 0.7



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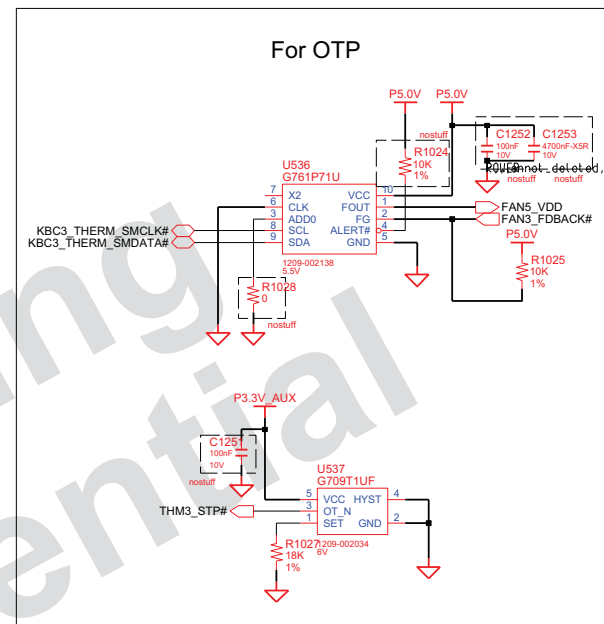
CLOCK DISTRIBUTION Rev. 0.8



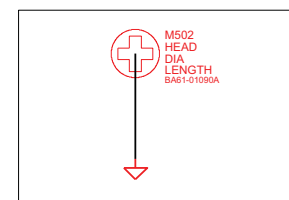
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APPROVAL	LEE, L	REV	REV 0.1	MAIN		
MODULE CODE	undefined	LAST EDIT	December, 17, 2012 12:15:06 PM	PAGE	5 OF 51	

b

THERMAL SENSOR & FAN CONTROL

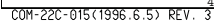


Temperature : 95.78c
confirmed by thermal charger
(2011.05.02)
 $R \text{ (kohm)} = 0.0012T - 0.9308T + 96.147$

FAN PEM

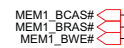
COM-22C-015(1996.6.5) REV. 3

IVYBRIDGE PROCESSOR (DMI,PEG, FDI)



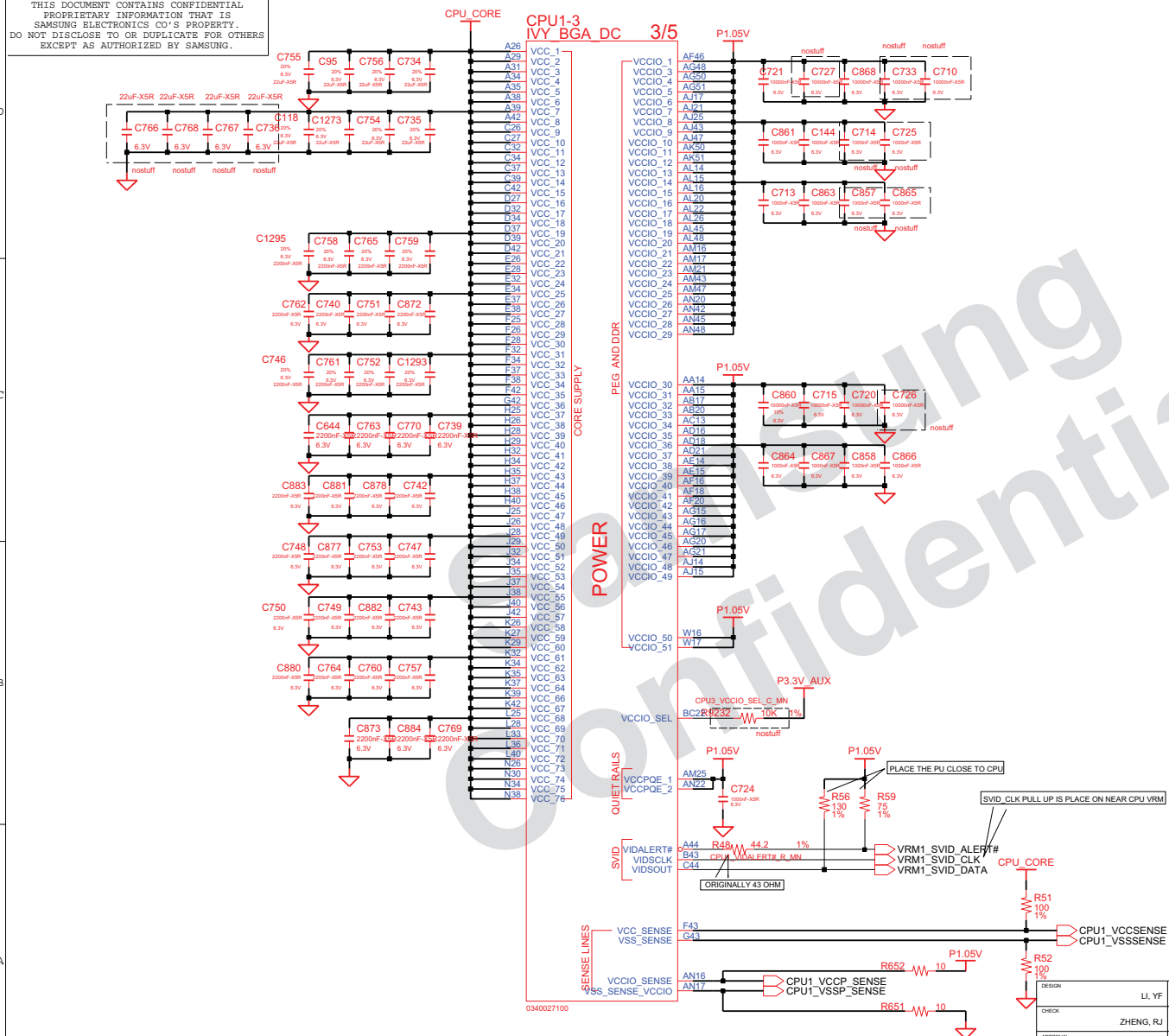
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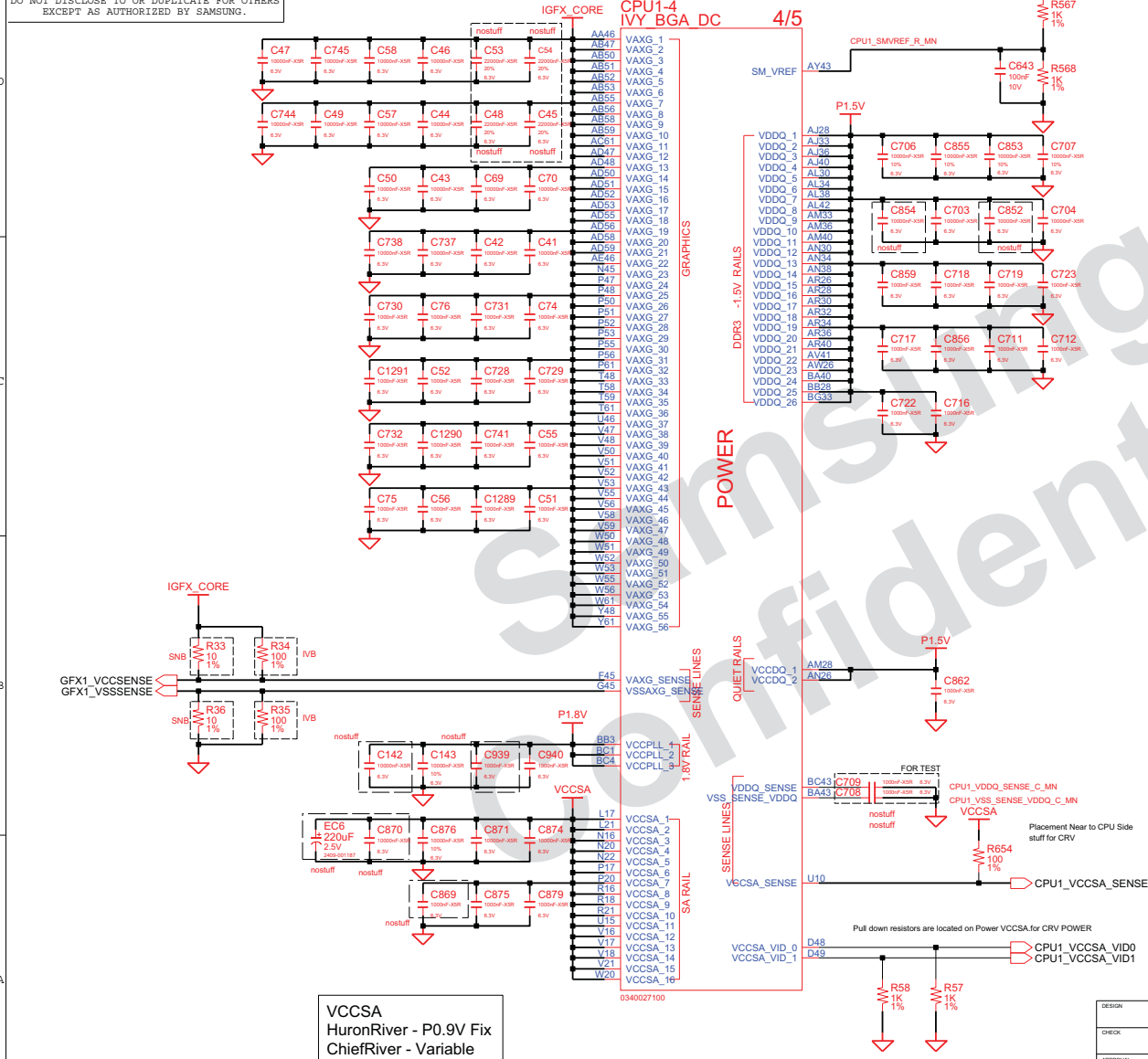
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APPROVAL	LEE, BL	REV	REV 0.1		BGA CPU (3/5)
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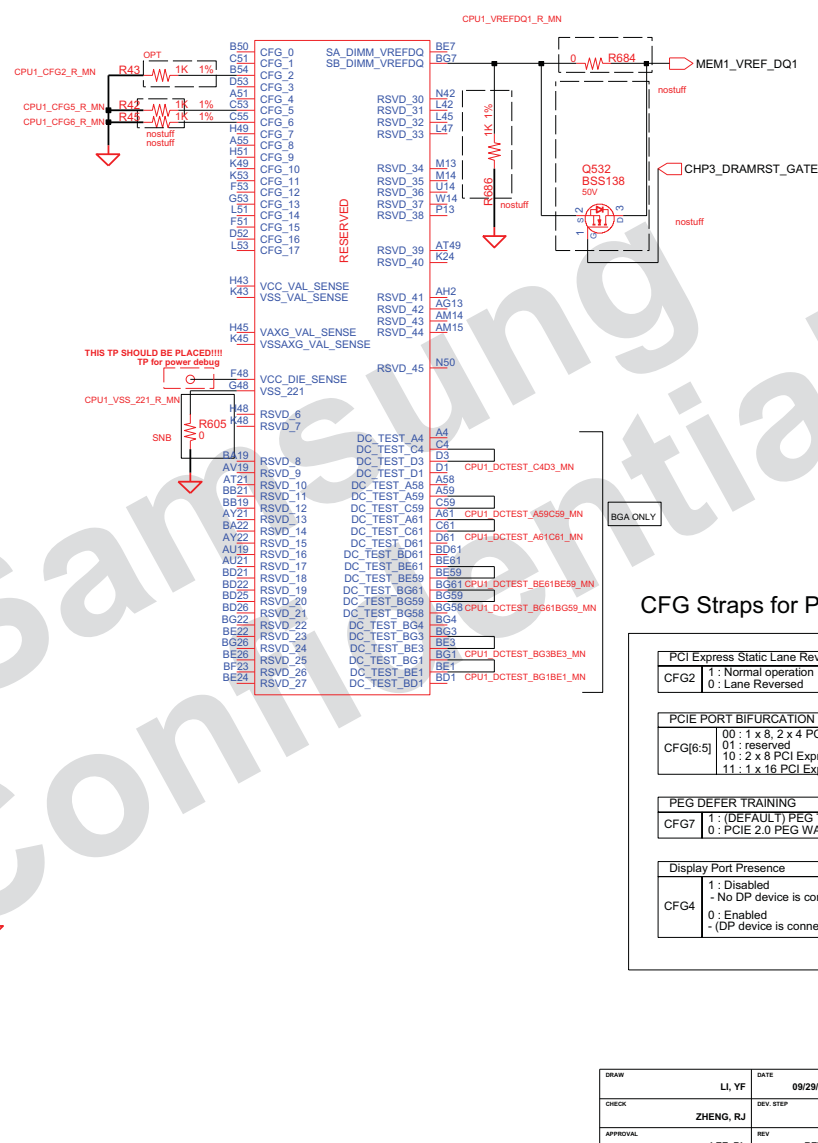
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VCCSA
HuronRiver - P0.9V Fix
ChiefRiver - Variable

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CHECK	ZHENG, RJ	REV. STEP	PVR		CPU	
APPROVAL	LEE, BL	REV	REV 0.1		BGA CPU (4/5)	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-*****A
December, 17, 2012 1:45:24 PM						PAGE 11 OF



PCI Express Static Lane Reversal	
CFG0	1: Normal operation 0: Lane Reversed

PCIe PORT BIFURCATION	
CFG0[6:5]	00: 1 x 8, 2 x 4 PCI Express 01: reserved 10: 2 x 8 PCI Express 11: 1 x 16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESET# DEASSERTION 0: PCIe 2.0 PEG WAIT FOR BIOS FOR TRAINING

Display Port Presence	
CFG0	1: Disabled - No DP device is connected to eDP 0: Enabled - (DP device is connected to eDP

COM-22C-015(1996.6.5) REV. 3

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DRAW	LI, YF	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG
CHECK	ZHENG, RJ	DEV. STEP	PVR		MEMORY #0 2 RANK(4/4)	ELECTRONICS
APPROVAL	LEE, L	REV	REV 0.1		DDR3 2Gb	PART NO. BA41-*****A
MODULE CODE	undefined	LAST EDIT	December, 17, 2012 1:47:16 PM	PAGE	13	OF 51

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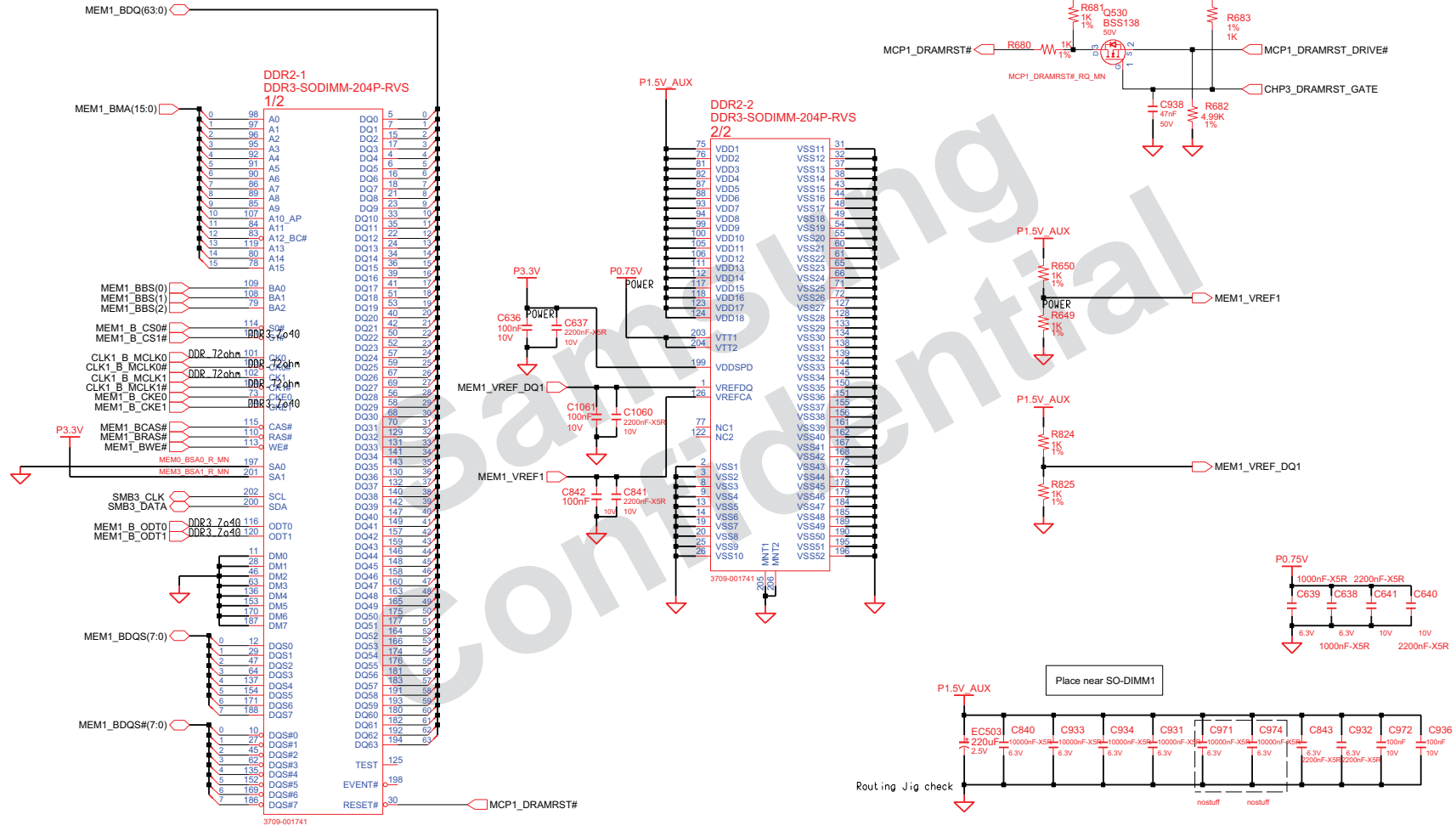
SO-DIMM #1 : 1st SO-DIMM

DDR SO-DIMM #1

Height : 8 mm (STANDARD)

P/N : 3709-001615 (FOXCONN)

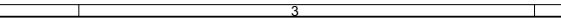
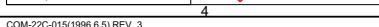
P/N : 3709-001622 (CONCRAFT)



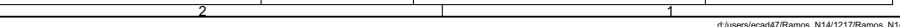
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CHECK	ZHENG, RJ	DEV. STEP	PVR		SODIMM B	
APPROVAL	LEE, BL	REV	REV 0.1		DDR3 2Gb	
MODULE CODE	undefined	LAST EDIT	December, 17, 2012 1:48:00 PM	PAGE	14 OF 51	

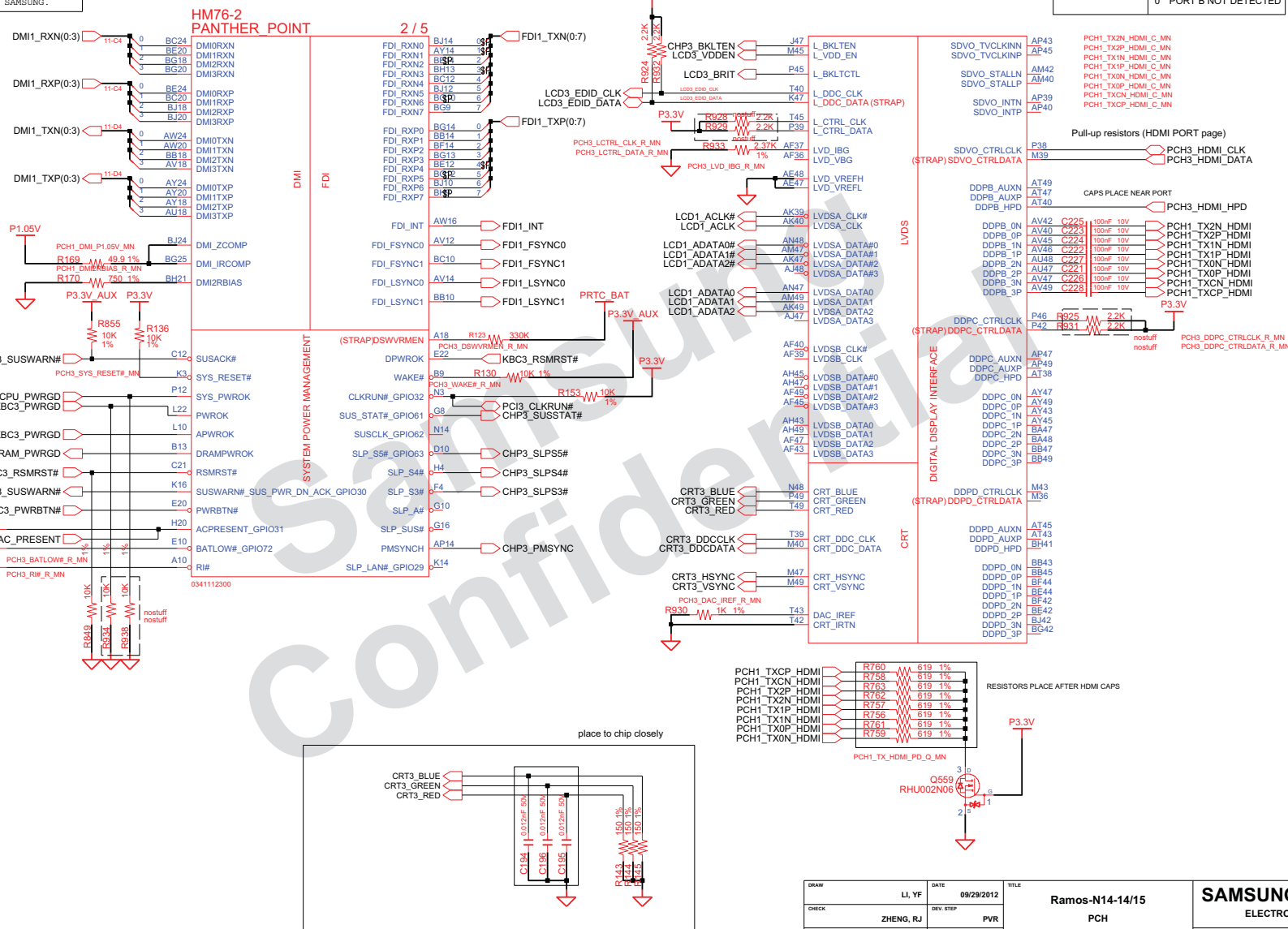
GPIO74 Function Definition		
0	R1044	NON_HSPA
1	R127	HSPA


GPIO67 Function Definition		
0	R1051	EXT
1	R1050	INT_OPT



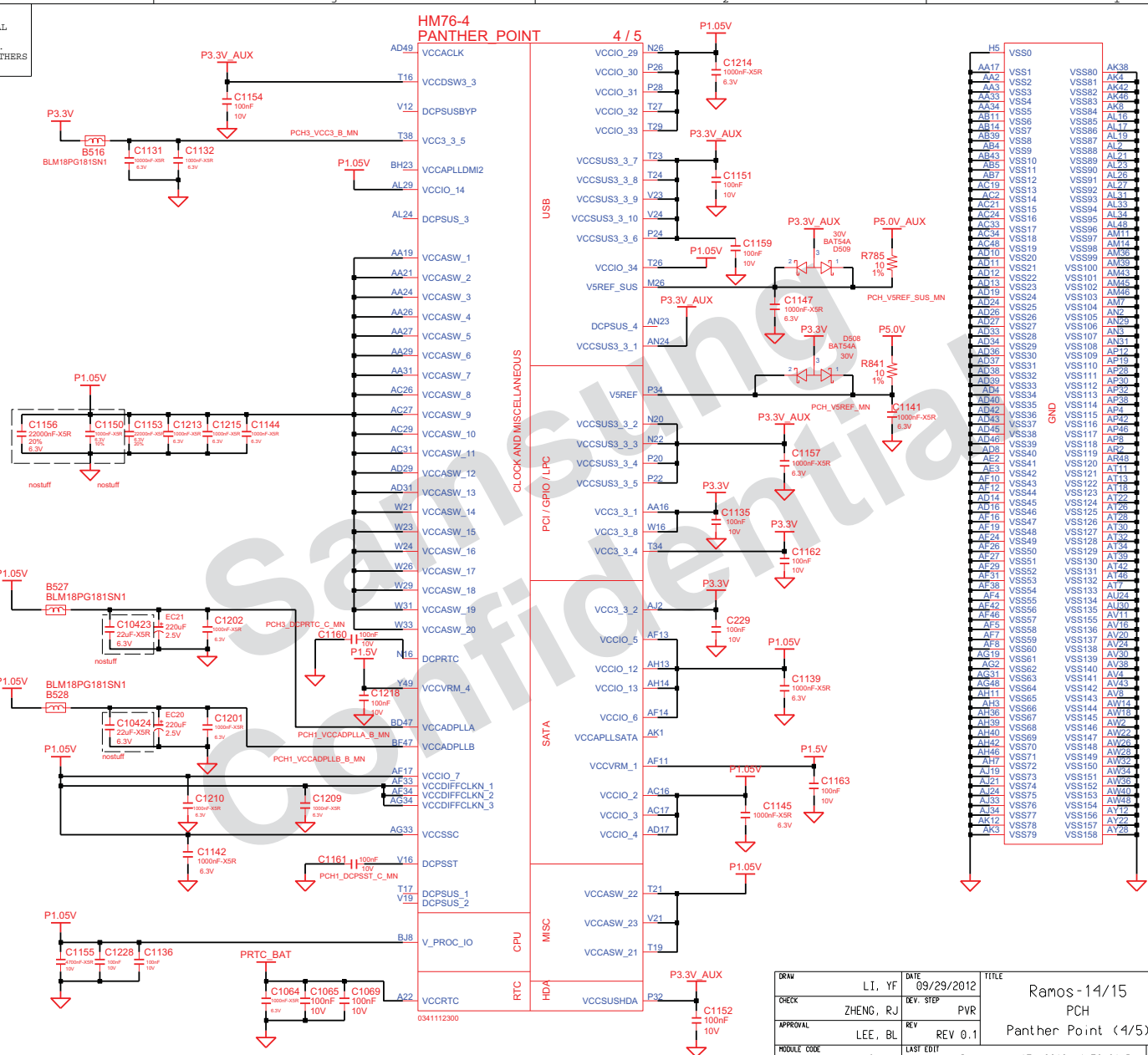
P3.3V





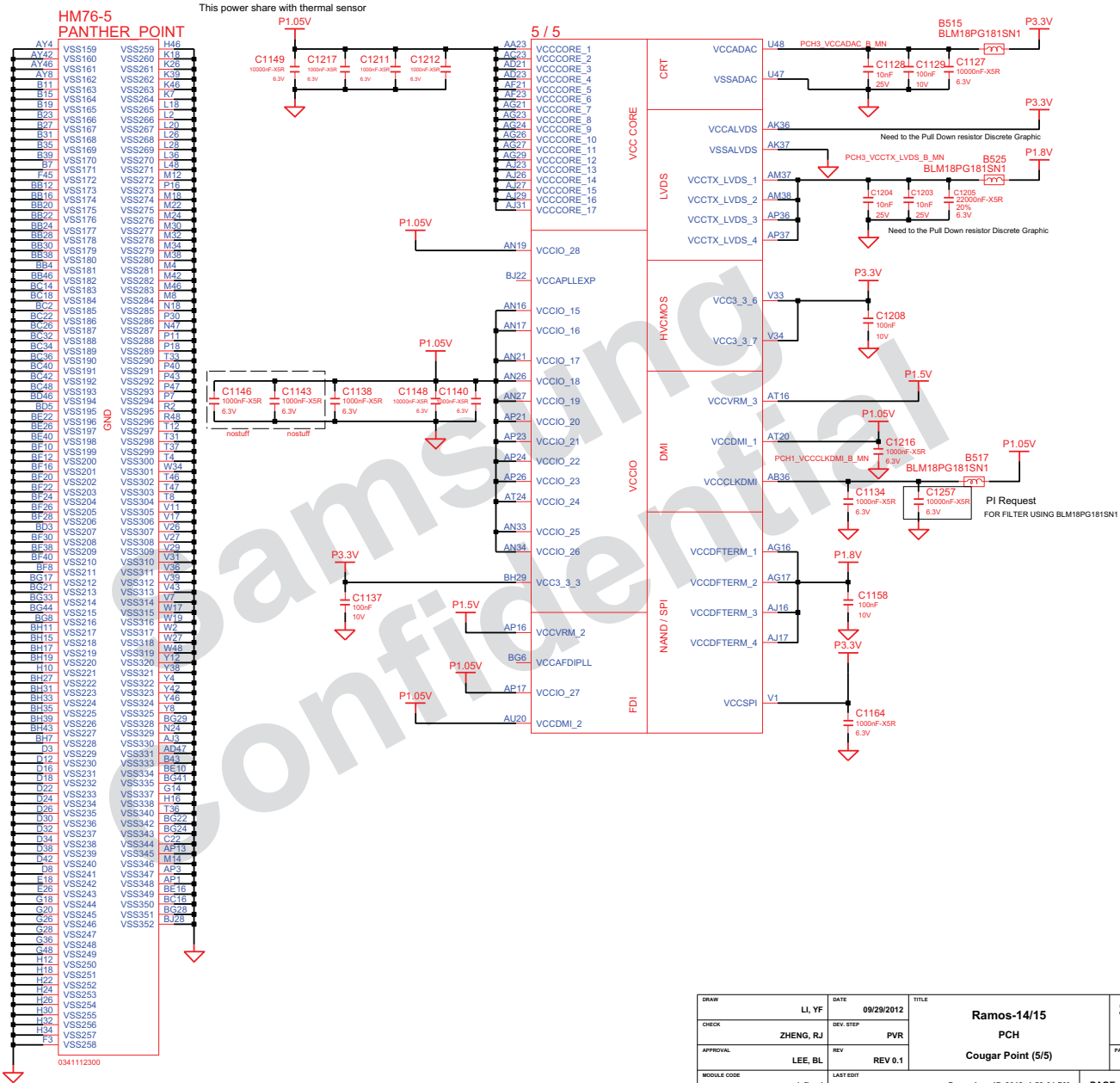
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APPROVAL	LEE, BL	REV	REV 0.1		
MODULE CODE	LAST EDIT				
December, 17, 2012 1:50:48 PM				PAGE	16 OF 51


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DRAW	L.I. YF	DATE	09/29/2012	TITLE	Ramos-14/15		SAMSUNG	
CHECK	ZHENG, R.J	REV. STEP	PVR		PCH		ELECTRONICS	
APPROVAL	LEE, BL	REV	REV 0.1		Panther Point (4/5)		PART NO.	BA41-*****A
MODULE CODE	undefined	LAST EDIT	December, 17, 2012 1:52:21 PM	PAGE	18	OF	51	

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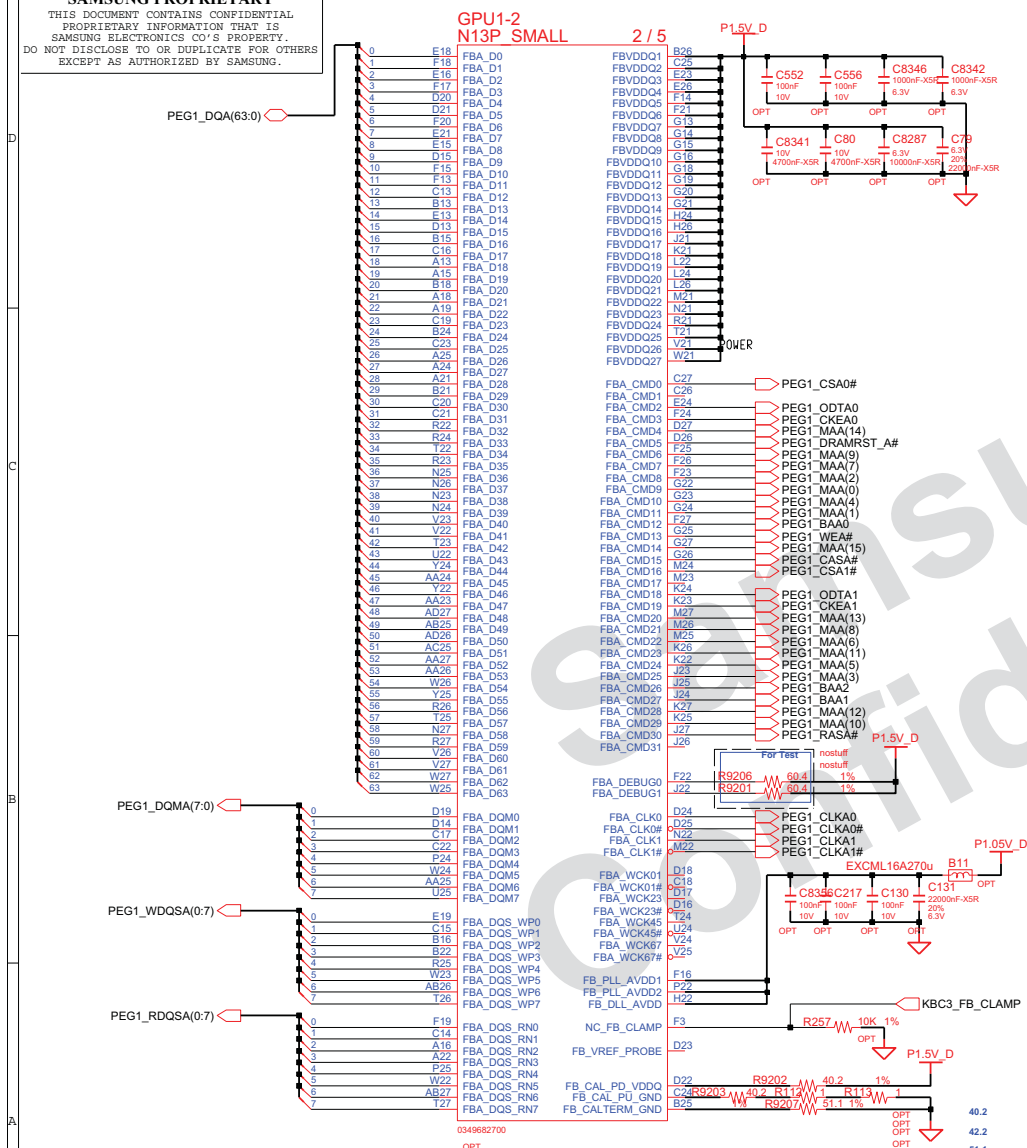



DRAW		LI, YF	DATE	09/29/2012	Ramos-14/15 PCH Cougar Point (5/5)				
CHECK		ZHENG, RJ	DEV. STEP	PVR			PART NO.		BA41-*****A
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MODULE CODE			LAST EDIT		December, 17, 2012 1:53:01 PM		PAGE	19 OF 51	

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DESIGN	LI, YF	DATE	1/27/2012	TITLE Ramos-N14-14/15 N14X_SMALL N14X (2/5)	
CHECK	ZHENG, RJ	DEV. STEP	PVR		
APPROVAL	LEE, BL	REV	REV 0.1		
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GPU1-3
N13P SMALL 3 / 5

IPFC_RSET		IPFC_AUX#	N5 N4
M7	IPFC_PLLVDD1	IPFC_L3#	N3
N7	IPFC_PLLVDD2	IPFC_L3#	N2
P6	IPFC_IOVDD	IPFC_L2#	R3
		IPFC_L2	R2
		IPFC_L1#	R1
		IPFC_L1	T1
		IPFC_L0#	T3
		IPFC_L0	T2
		IPFC_L0	T4
		GPIO15	C3
U6	IPFD_RSET	IPFD_AUX#	P4
		IPFD_AUX	P3
T7	IPFD_PLLVDD1	IPFD_L3#	R5
R7	IPFD_PLLVDD2	IPFD_L3#	R4
R6	IPFD_IOVDD	IPFD_L2#	T5
		IPFD_L2	T4
		IPFD_L1#	U4
		IPFD_L1	U3
		IPFD_L0#	V4
		IPFD_L0	V3
		IPFD_L0	V2
		GPIO17	D4
J7	IPFEF_PLLVDD1	IPFEF_AUX#	J3
K7	IPFEF_PLLVDD2	IPFEF_AUX	J2
K6	IPFEF_RSET	IPFEF_L3#	J1
		IPFEF_L3	K1
		IPFEF_L2#	K3
		IPFEF_L2	K2
		IPFEF_L1#	M3
		IPFEF_L1	M1
		IPFEF_L0#	N1
		IPFEF_L0	N2
		GPIO18	C2
H6	IPFEF_IOVDD	IPFEF_AUX#	H4
		IPFEF_AUX	H3
J6	IPFF_IOVDD	IPFF_L3#	J5
		IPFF_L3	J4
		IPFF_L2#	K5
		IPFF_L2	K4
		IPFF_L1#	L5
		IPFF_L1	L4
		IPFF_L0#	M5
		IPFF_L0	M4
		IPFF_L0	M3
		GPIO19	F7

0349682700

OPT

DESIGN	LI, YF	DATE	1/27/2012	TITLE		SAMSUNG ELECTRONICS	
CHECK	ZHENG, RJ	REV. STEP	PVR				
APPROVAL	LEE, BL	REV	REV 0.1	Ramos-N14-14/15 N14X_SMALL N14X(3/5)		PART NO.	BA41-xxxxxx
MODULE CODE	undefined		LAST EDIT		December, 17, 2012 1:58:24 PM	PAGE	22 OF 51

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CHECK		ZHENG, RJ	DEV. STEP	PVR		PART NO. BA41-xxxxxx			
APPROVAL		LEE, BL	REV	REV 0.1					
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						PAGE	23	OF	51

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GF117_N14M_GL/GE STRAP DEFINITION

GK208_N14M_LP/GS STRAP DEFINITION

GK208_N14P_GV2 STRAP DEFINITION

RESISTOR MAPPING TO HEX VALUES

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU STRAP TABLE

STRAP PIN	GK208			GF117			VRAM	GPU
	N14P_GV2	N14M_GS	N14M_LP	N14M_GE	N14M_GL	N14M_GL		
ROM_SCLK	5K PU LP_GS_GV2	5K PU LP_GS_GV2	5K PU LP_GS_GV2	10K PD GL_GE	10K PD GL_GE	10K PD GL_GE	SAM1G	N14M-GL
ROM_SI	refer to RAM strap	refer to RAM strap	refer to RAM strap	10K PD GL_GE	10K PD GL_GE	10K PD GL_GE	SAM2G	N14M-GE
ROM_SO	5K PU LP_GS_GV2	5K PU LP_GS_GV2	5K PU LP_GS_GV2	10K PD GL_GE	10K PD GL_GE	10K PD GL_GE	HY1G	N14M-LP
STRAP0	45K PU LP_GS_GV2	45K PU LP_GS_GV2	45K PU LP_GS_GV2	refer to RAM strap	refer to RAM strap	refer to RAM strap	HY2G	N14M-GS
STRAP1	45K PD LP_GS_GV2	45K PD LP_GS_GV2	45K PD LP_GS_GV2	refer to RAM strap	refer to RAM strap	refer to RAM strap	MICRO1G	N14P-GV2
STRAP2	15K PD GV2	5K PD GS	10K PD LP	refer to RAM strap	refer to RAM strap	refer to RAM strap	MICRO2G	
STRAP3	5K PD LP_GS_GV2	5K PD LP_GS_GV2	5K PD LP_GS_GV2	refer to RAM strap	refer to RAM strap	refer to RAM strap		
STRAP4	45K PD LP_GS_GV2	45K PD LP_GS_GV2	45K PD LP_GS_GV2	10K PD GL_GE	10K PD GL_GE	10K PD GL_GE		

MULTI-LEVEL MODE STRAPPING

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN	PCIE_MAX_SPEED	DP_PLL_VDD33V

BINARY STRAP

STRAP PIN	STRAP MAPPING	RESISTANCE	POLARITY
ROM_SCLK	SMB_ALT_ADDR	10K	PD
ROM_SI	SUB_VENDOR	10K	PU TO 3V3 IF VBIOS ROM EXISTS PD IF NO VBIOS ROM EXISTS
ROM_SO	VGA_DEVICE	10K	PD(NO DISPLAY)
STRAP0	RAM_CFG[0]	10K	NA
STRAP1	RAM_CFG[1]	10K	NA
STRAP2	RAM_CFG[2]	10K	NA
STRAP3	RAM_CFG[3]	10K	NA
STRAP4	PCIE_MAX_SPEED	10K	PD

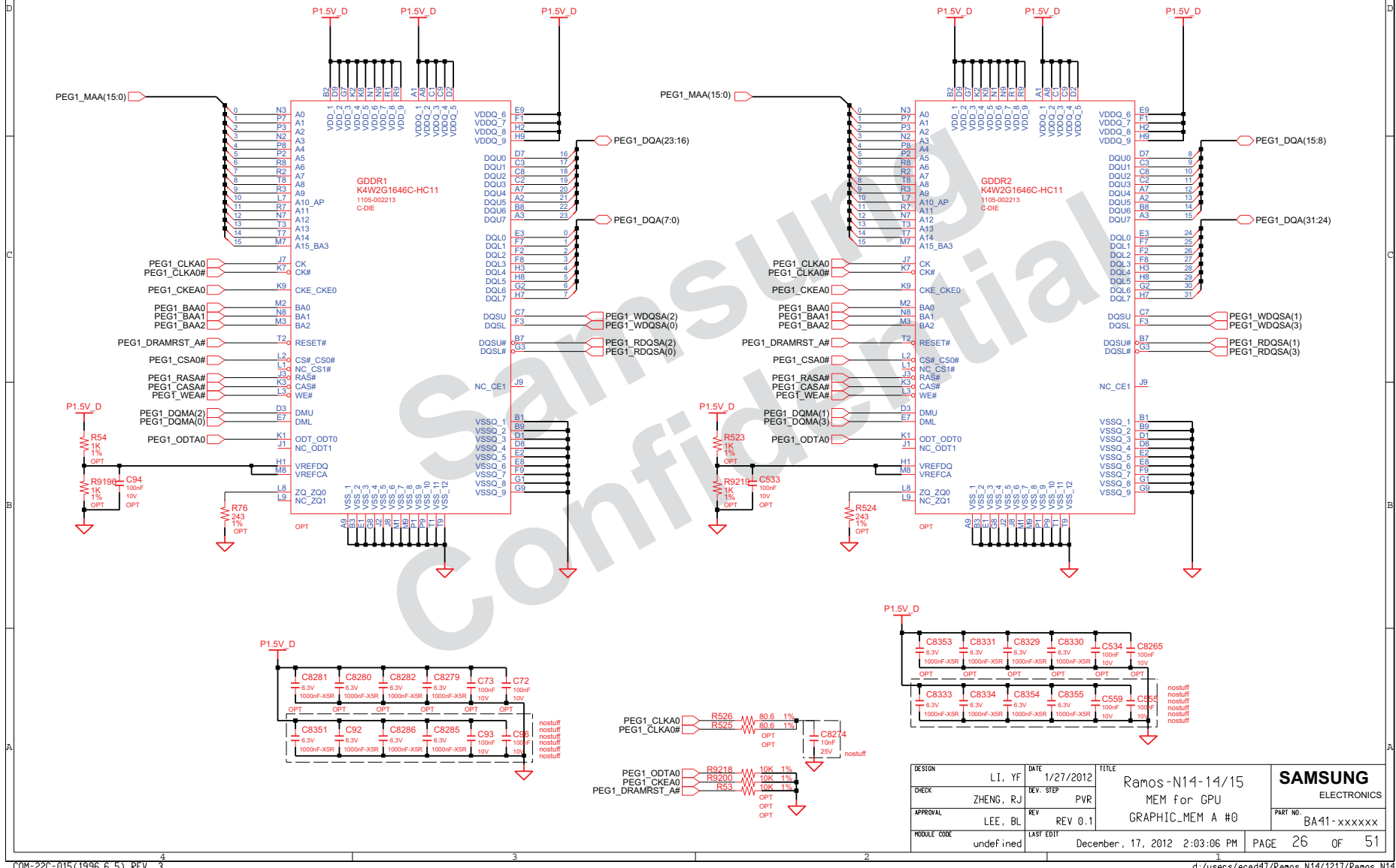
VRAM STRAP TABLE

	SAM 1G	SAM 2G	HY 1G	HY 2G	MICRO 1G	MICRO 2G
GK208 ROM_SI	LP_GS_GV2_1G 45K PD	LP_GS_GV2_2G 20K PD	LP_GS_GV2_1G 35K PD	NA	LP_GS_GV2_1G 30K PD	LP_GS_GV2_2G 10K PD
GF117 STRAP0	SAM_MICRO_1G 10K PU	SAM_HY_MICRO_2G 10K PU	HY_1G 10K PD	SAM_HY_MICRO_2G 10K PU	SAM_MICRO_1G 10K PU	SAM_HY_MICRO_2G 10K PU
GF117 STRAP1	SAM_MICRO_1G 10K PD	SAM_HY_2G 10K PU	HY_1G 10K PU	SAM_HY_2G 10K PU	SAM_MICRO_1G 10K PD	MICRO_2G 10K PD
GF117 STRAP2	SAM_HY_1G 10K PU	SAM_HY_2G 10K PD	SAM_HY_1G 10K PU	SAM_HY_2G 10K PD	MICRO_1G 10K PD	MICRO_2G 10K PU
GF117 STRAP3	SAM_HY_MICRO_1G 10K PD	SAM_MICRO_2G 10K PU	SAM_HY_MICRO_1G 10K PD	HY_2G 10K PD	SAM_HY_MICRO_1G 10K PD	SAM_MICRO_2G 10K PU

DESIGN	LL YF	DATE	1/27/2012	TITLE	Ramos-N14-14/15	SAMSUNG
CHECK	ZHENG, RJ	DEV. STEP	PVR		N14X_SMALL	ELECTRONICS
APPROVAL	LEE, BL	REV	REV 0.1		GRAPHIC STRAP	PART NO.
MODULE CODE	undefined	LAST EDIT				BA41-xxxxxx
				December, 17, 2012 2:02:10 PM	PAGE	25 OF 51

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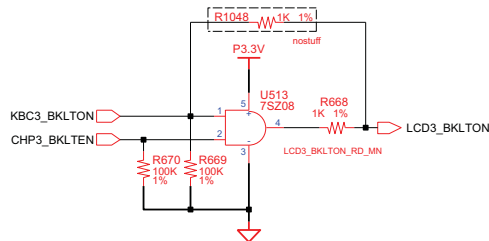
A-Channel #0 (D-mode)



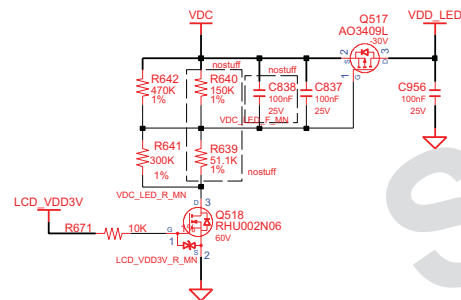
DESIGN	LI, YF	DATE	1/27/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS
CHECK	ZHENG, RJ	DEV. STEP	PVR		MEM for GPU	
APPROVAL	LEE, BL	REV	REV 0.1		GRAPHIC.MEM A #0	PART NO. BA41-xxxxxx
MOBILE CODE	undefined	LAST EDIT	December, 17, 2012 2:03:06 PM			PAGE 26 OF 51

LVDS LOGIC

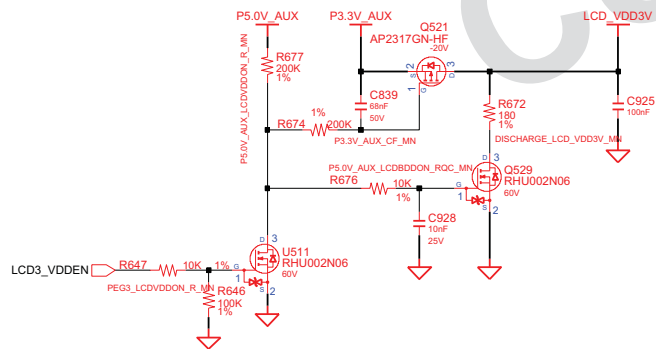
Backlight On



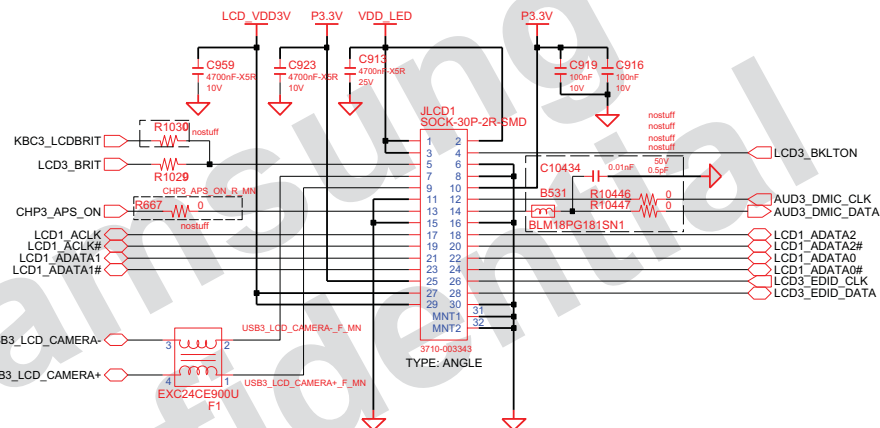
LED Power



LCD Power



1Ch. LCD Connector + CAMERA + INT MIC

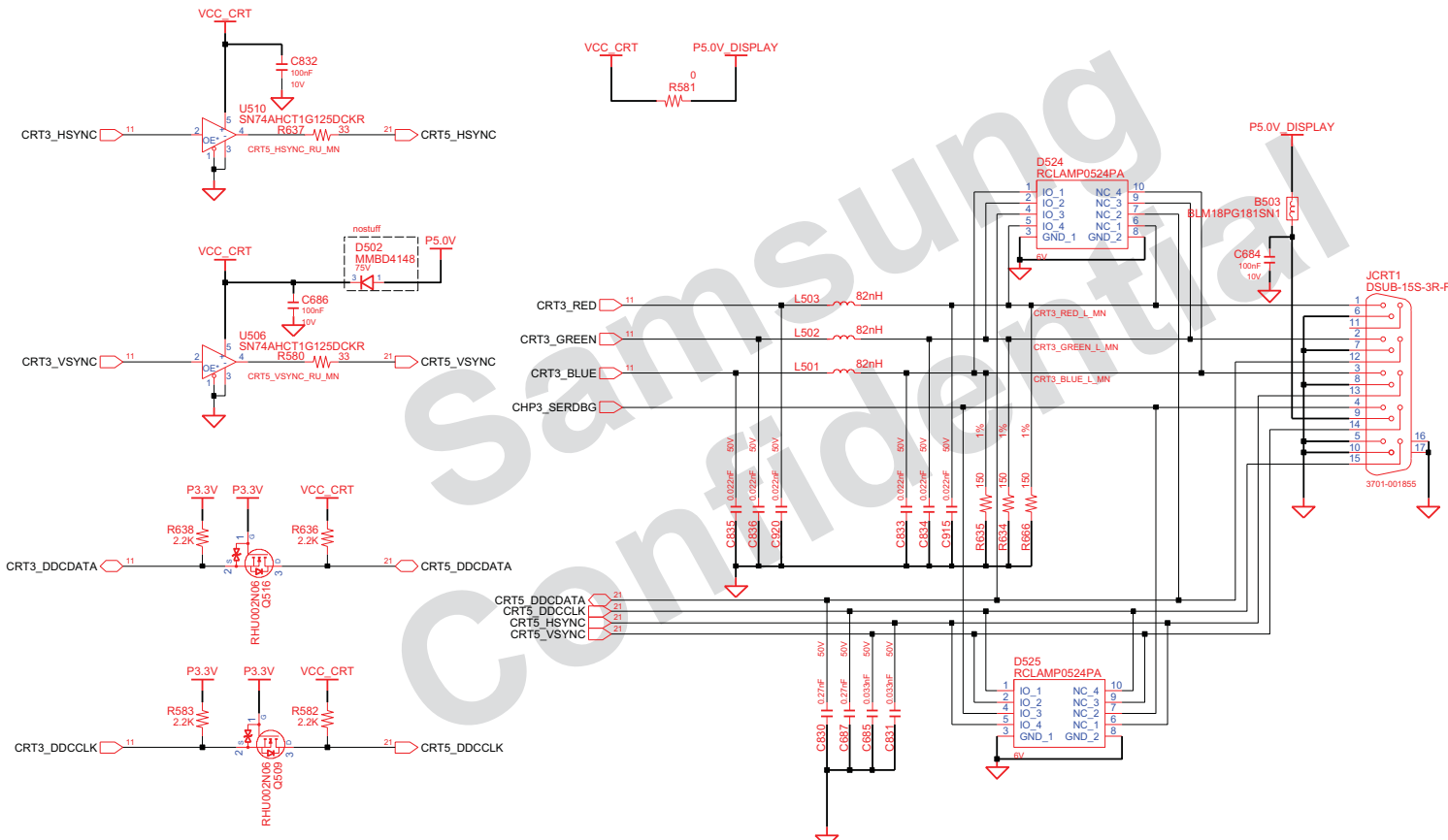


USB signal stub should be less than 100mil

DESIGN	LI, YF	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	ZHENG, RJ	DEV. STEP	PVR	GRAPHICS_If		
APPROVAL	LEE, BL	REV	REV 0.1	LVDS		
MODULE CODE	undefined	LAST EDIT				
December, 17, 2012 2:05:09 PM						PAGE 28 OF 51

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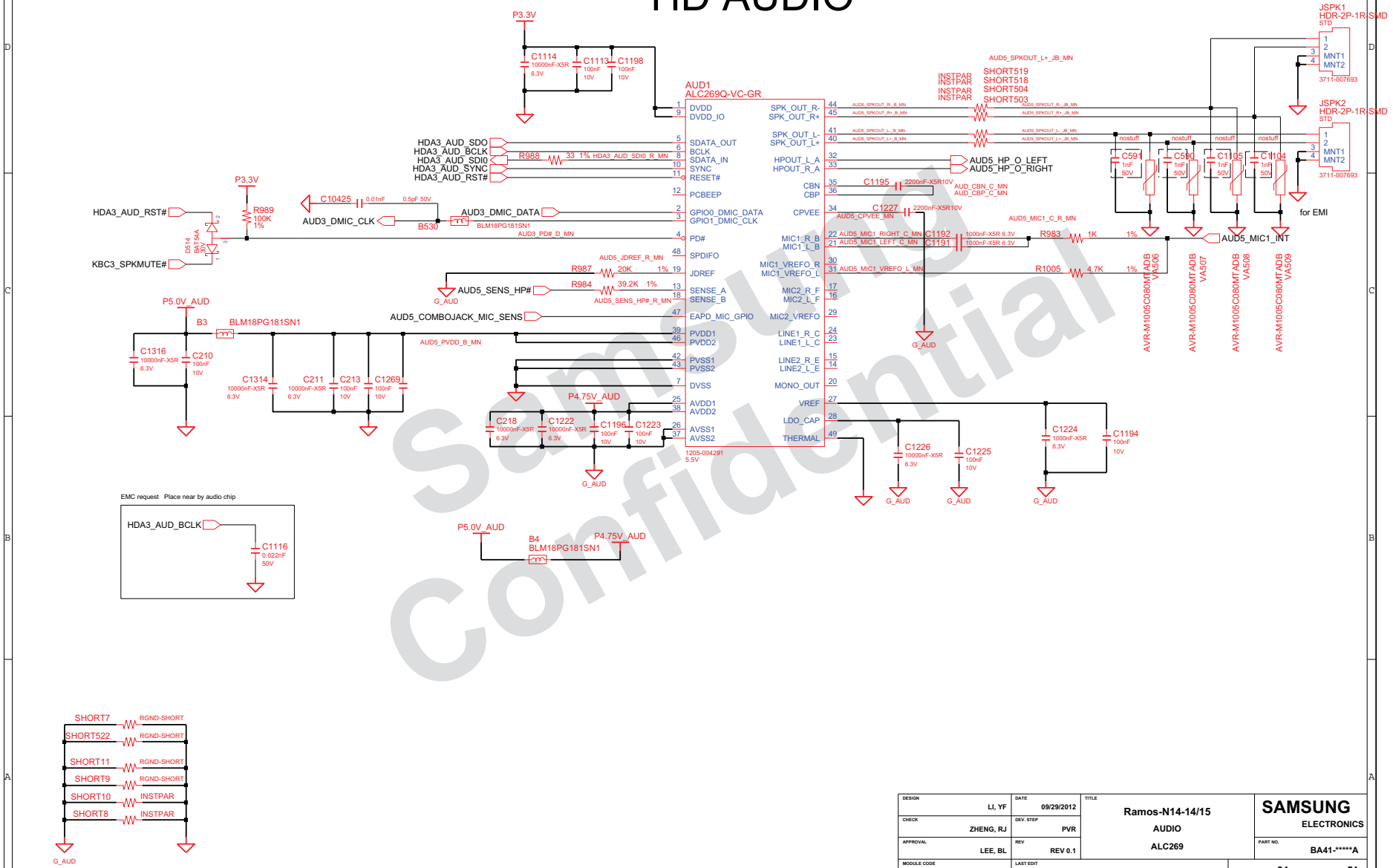
VGA



DESIGN	LI, YF	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG ELECTRONICS PART NO. BA41-*****A
CHECK	ZHENG, RJ	DEV. STEP	PVR	GRAPHIC_IF	CRT	
APPROVAL	LEE, BL	REV	REV 0.1			
MODULE CODE	undefined	LAST EDIT	December, 17, 2012 2:05:49 PM	PAGE	29 OF 51	

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HD AUDIO



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TID AUDIO



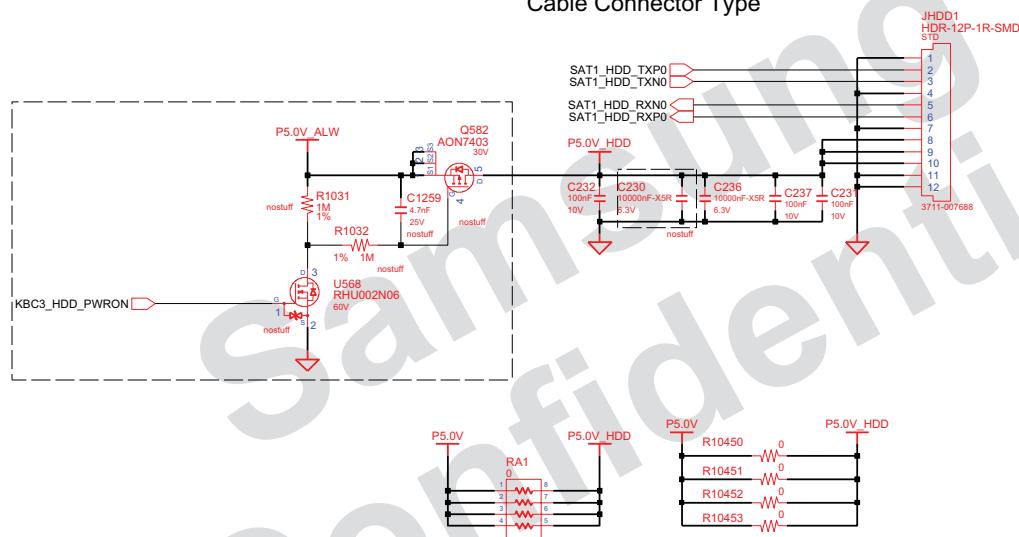
COM-22C-015(1996 6 5) RFV	4	3	2	1
				d:\users\acad47\Ramos_N14\1217\Ramos_N1

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SATA I/F CONN

SATA HDD CONN

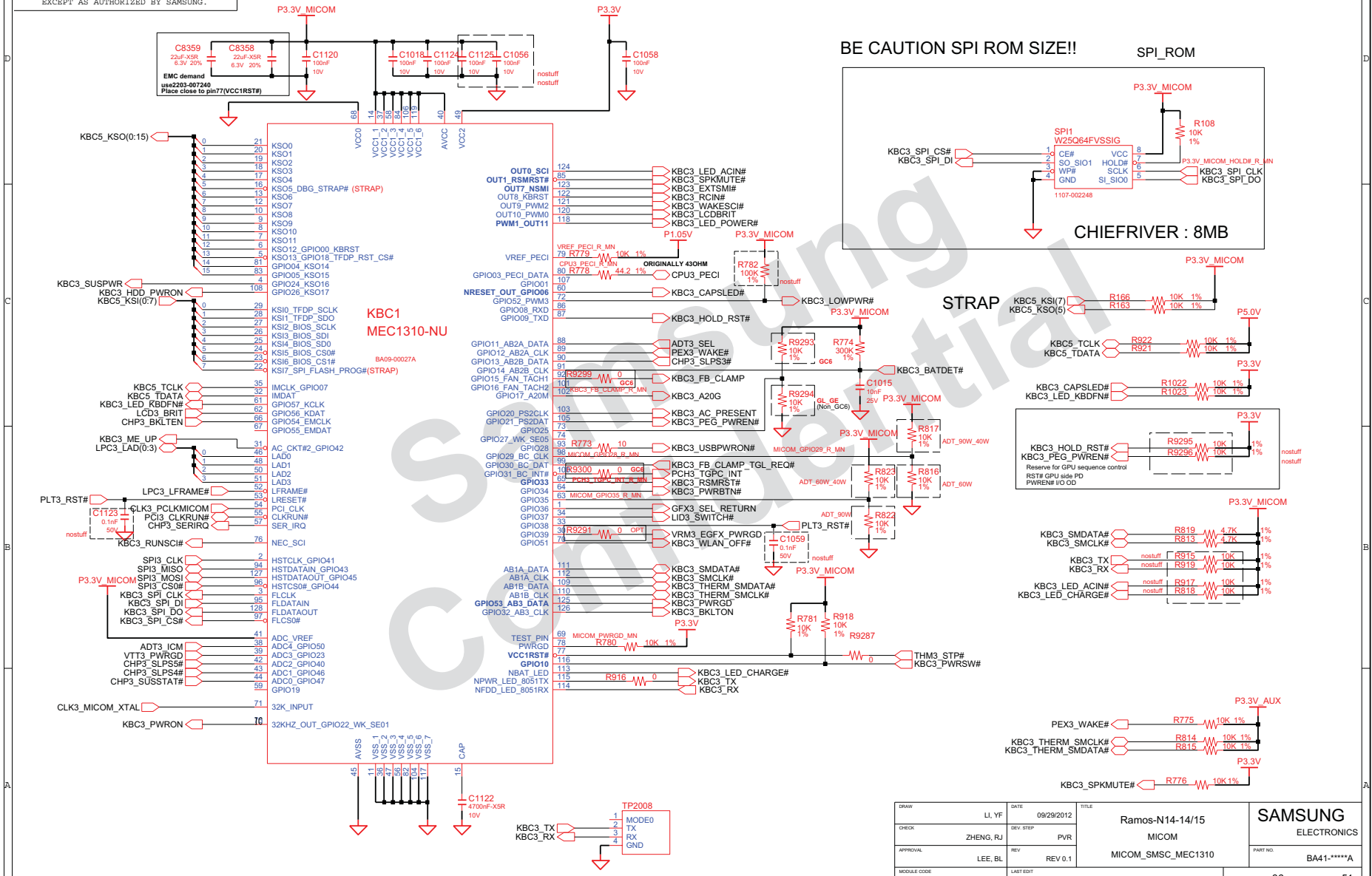
Cable Connector Type



DESIGN	LI, YF	DATE	09/29/2012	Ramos-N14-14/15 SATA I/F SATA I/F		SAMSUNG ELECTRONICS PART NO. BA41-*****A					
CHECK	ZHENG, RJ	DEV. STEP	PVR								
APPROVAL	LEE, BL	REV	REV 0.1								
MODULE CODE		undefined		LAST EDIT		December, 17, 2012 2:10:21 PM		PAGE	35	OF	51

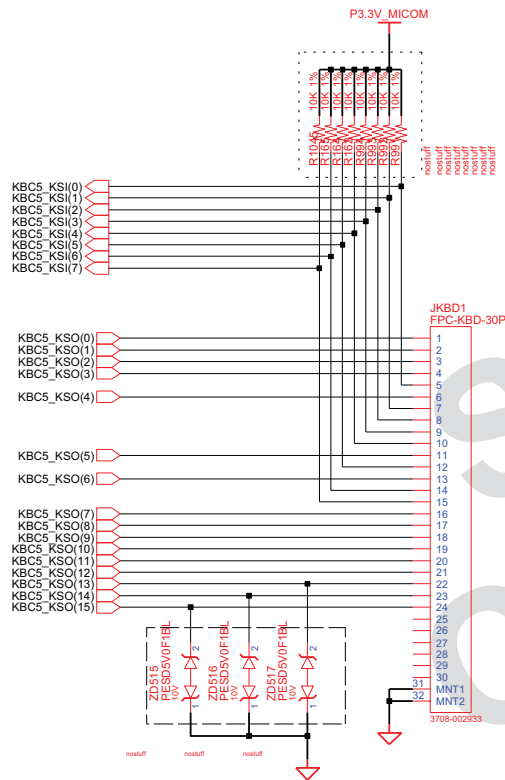
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MAIN BOARD (MICOM)

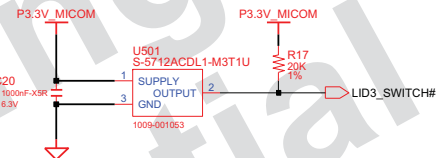


Micom Glue

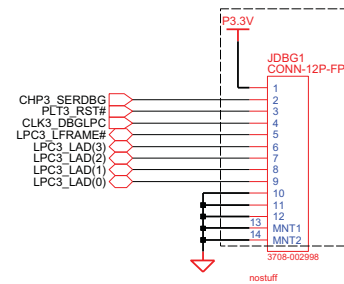
KEYBOARD



LID3_SWITCH



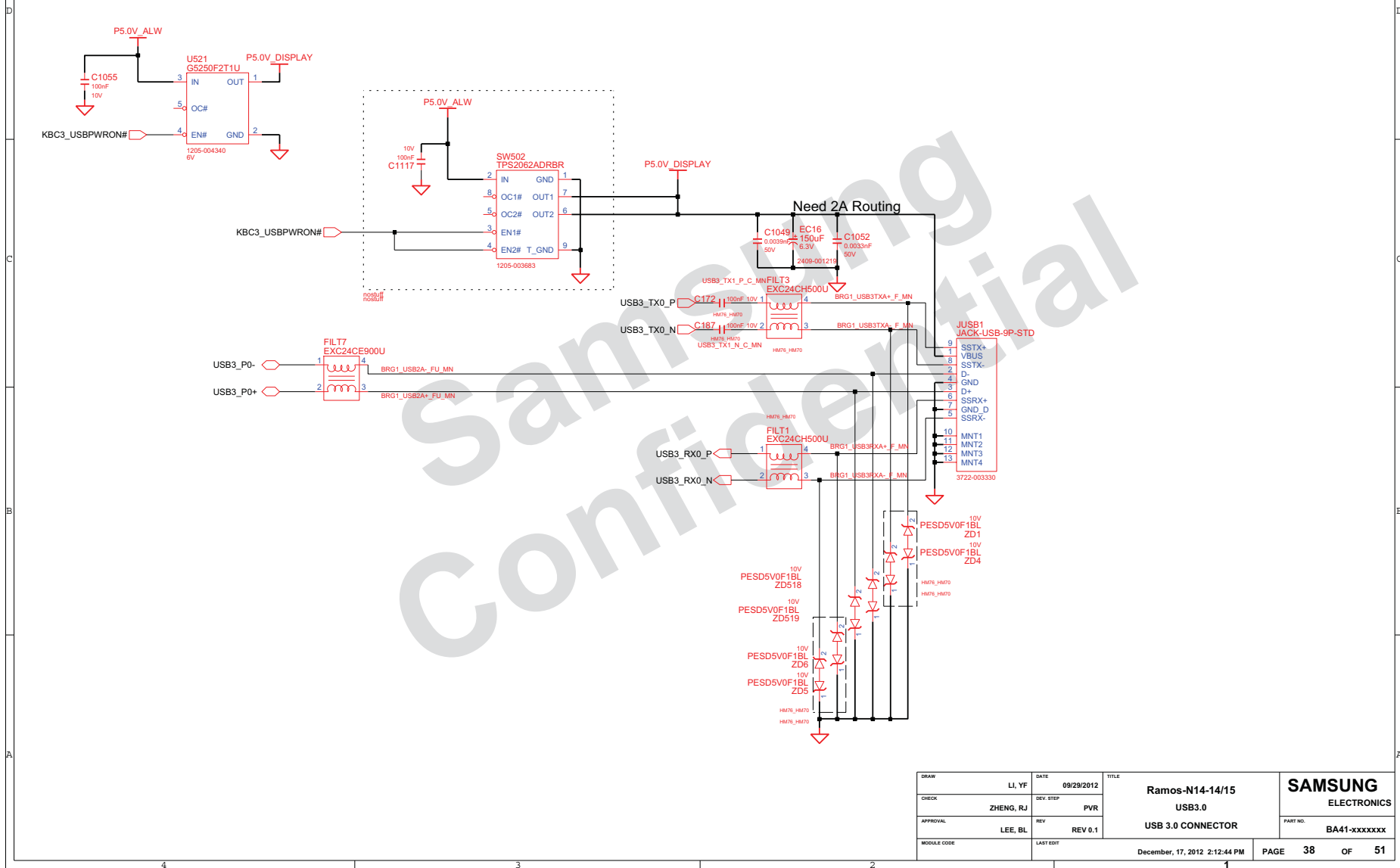
80H PORT DEBUG



DRAW	LI, YF	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS
CHECK	ZHENG, RJ	DEV. STEP	PVR		MICOM	
APPROVAL	LEE, BL	REV	REV 0.1		MICOM GLUE LOGIC	
MODULE CODE		LAST EDIT				
December, 17, 2012 2:11:59 PM						PAGE 37 OF 51

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USB 3.0 CONNECTOR



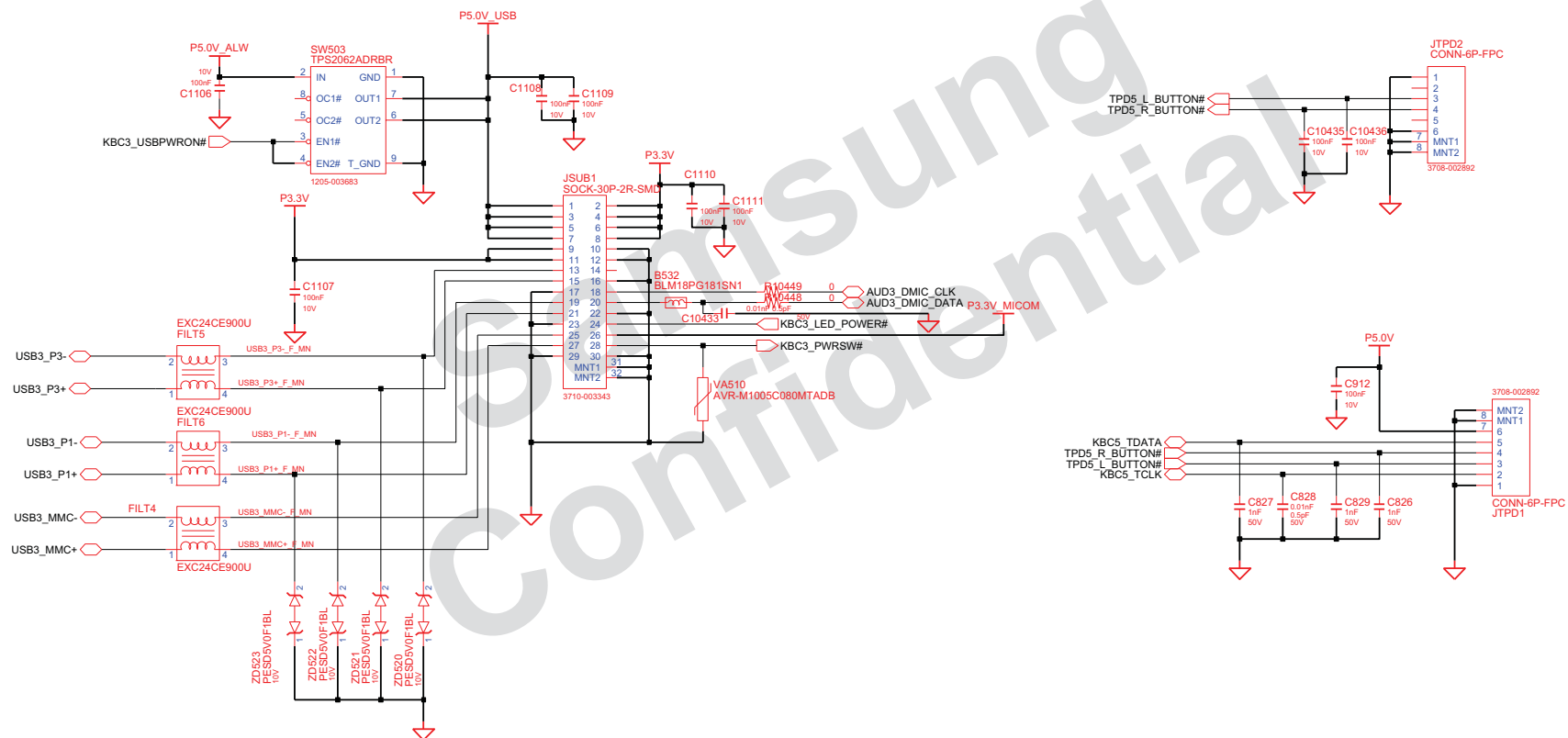
DRAW	LI, YP	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS
CHECK	ZHENG, RJ	DEV. STEP	PVR		USB3.0	
APPROVAL	LEE, BL	REV	REV 0.1		USB 3.0 CONNECTOR	PART NO. BA41-xxxxxxx
MODULE CODE		LAST EDIT		December, 17, 2012 2:12:44 PM	PAGE 38 OF 51	

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MAIN TO SUB

MAIN to 3-in-1 / USB SUB

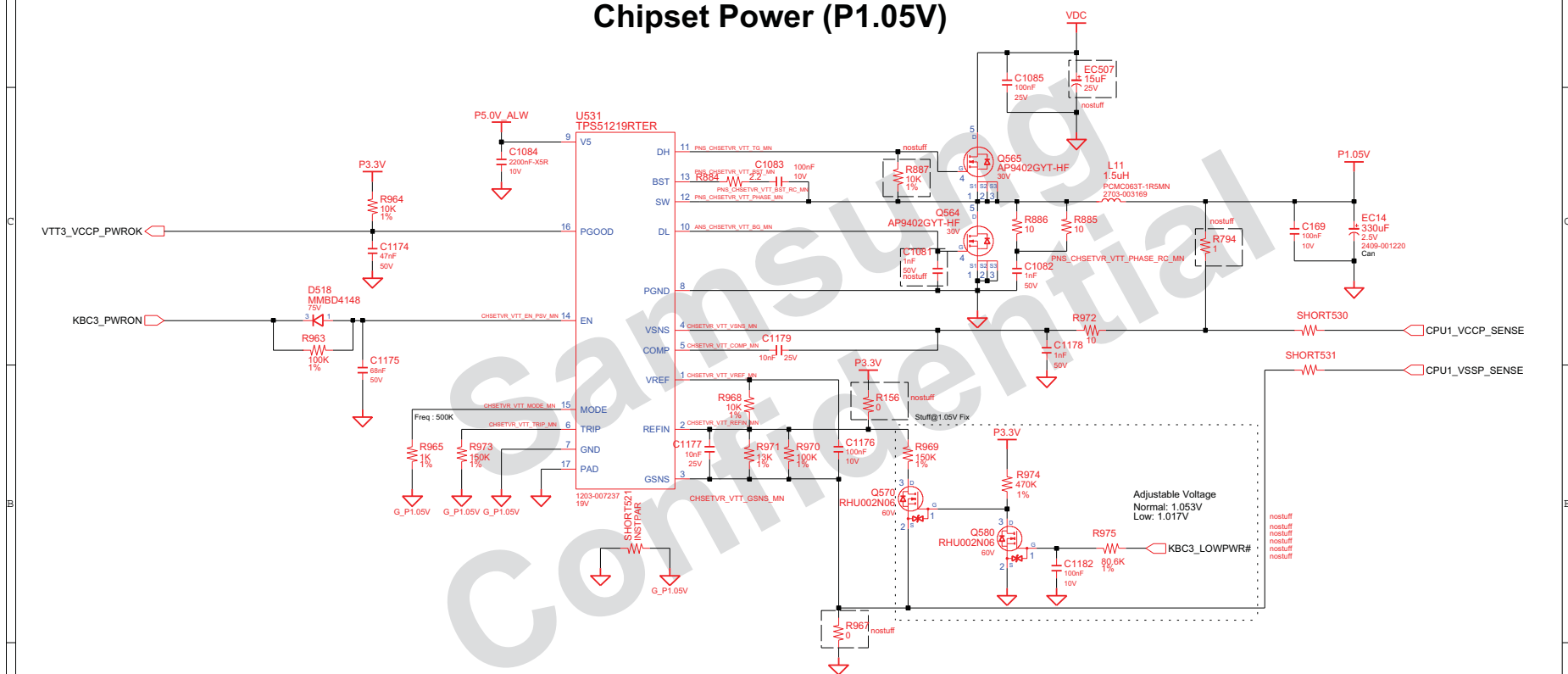
TOUCHPAD BUTTON MAIN TO SUB



DESIGN	LI, YF	DATE	09/29/2012	TITLE	Ramos-N14-14/15	SAMSUNG ELECTRONICS
CHECK	ZHENG, RJ	REV. STEP	PVR	SUB BOARD CONNECTOR		
APPROVAL	LEE, BL	REV	REV 0.1	MAIN TO SUB	PART NO.	BA41-*****A
MOBILE CODE	undefined	LAST EDIT		December, 17, 2012 2:13:27 PM	PAGE	39 OF 51

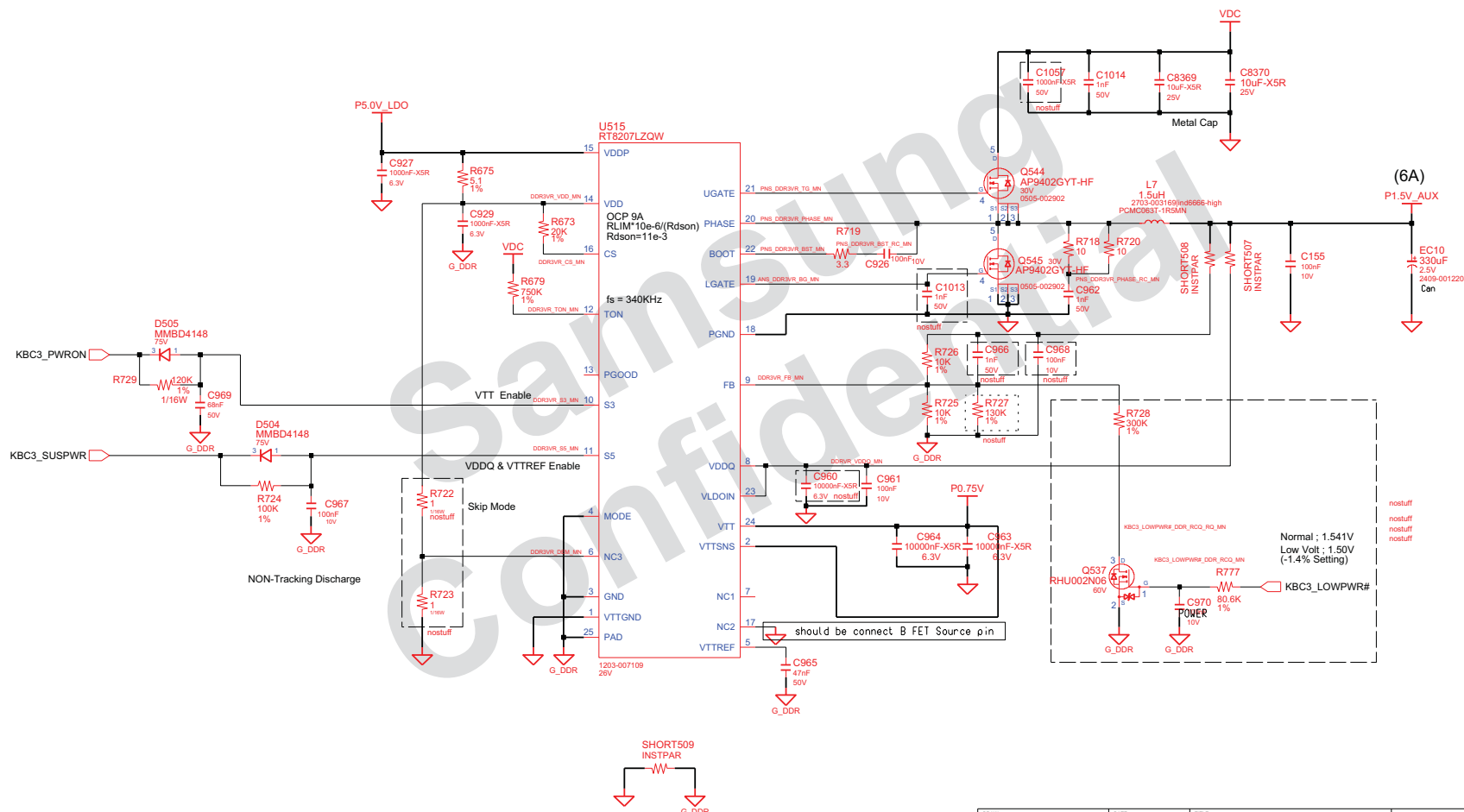
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Chipset Power (P1.05V)



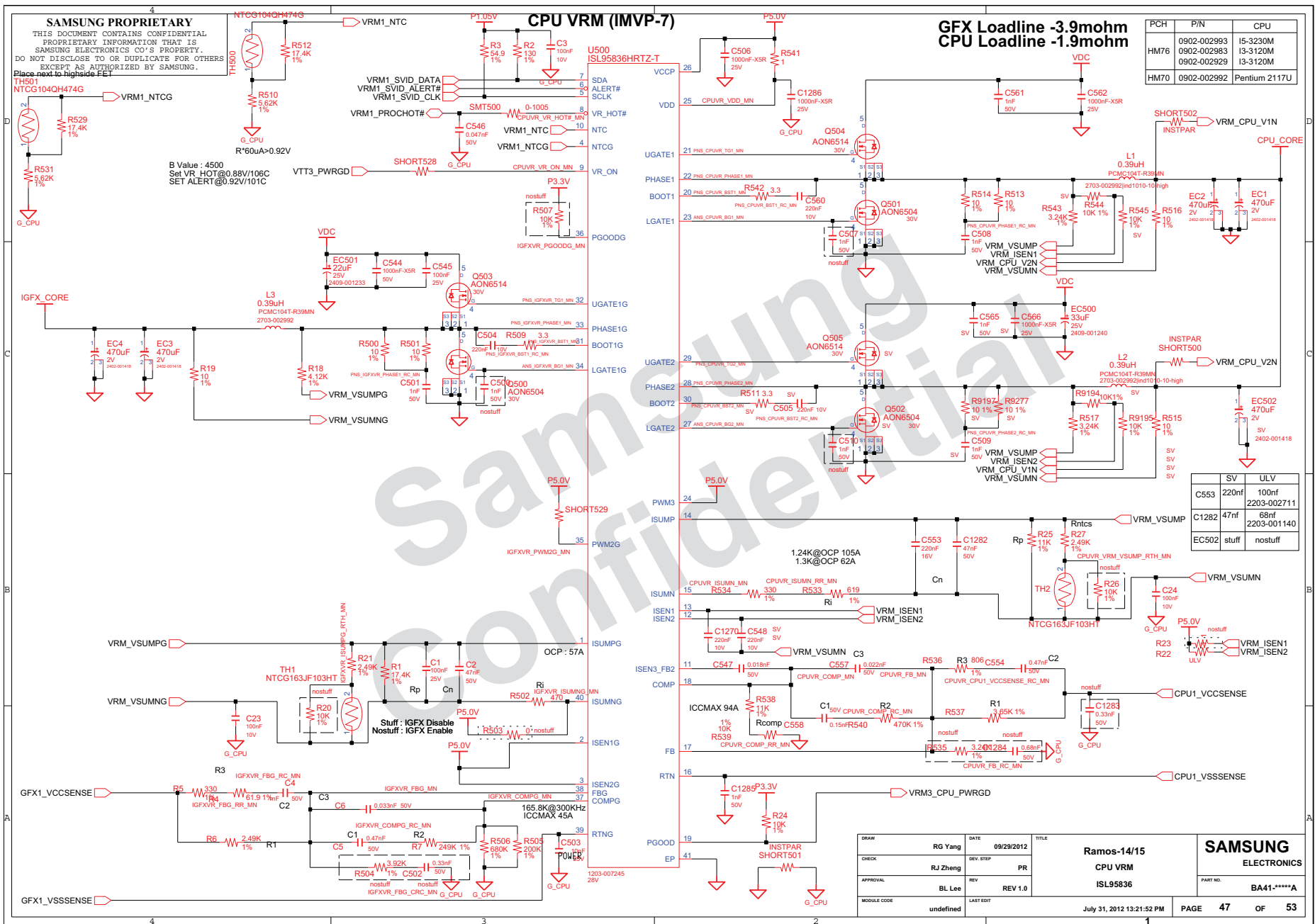
DESIGN	RG Yang	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		CHIPSET PWR	
APPROVAL	BL Lee	REV	REV 1.0		P1.05V	
MODULE CODE		LAST EDIT				
July 31, 2012 13:21:52 PM						PAGE 44 OF 53

DDR3 Power



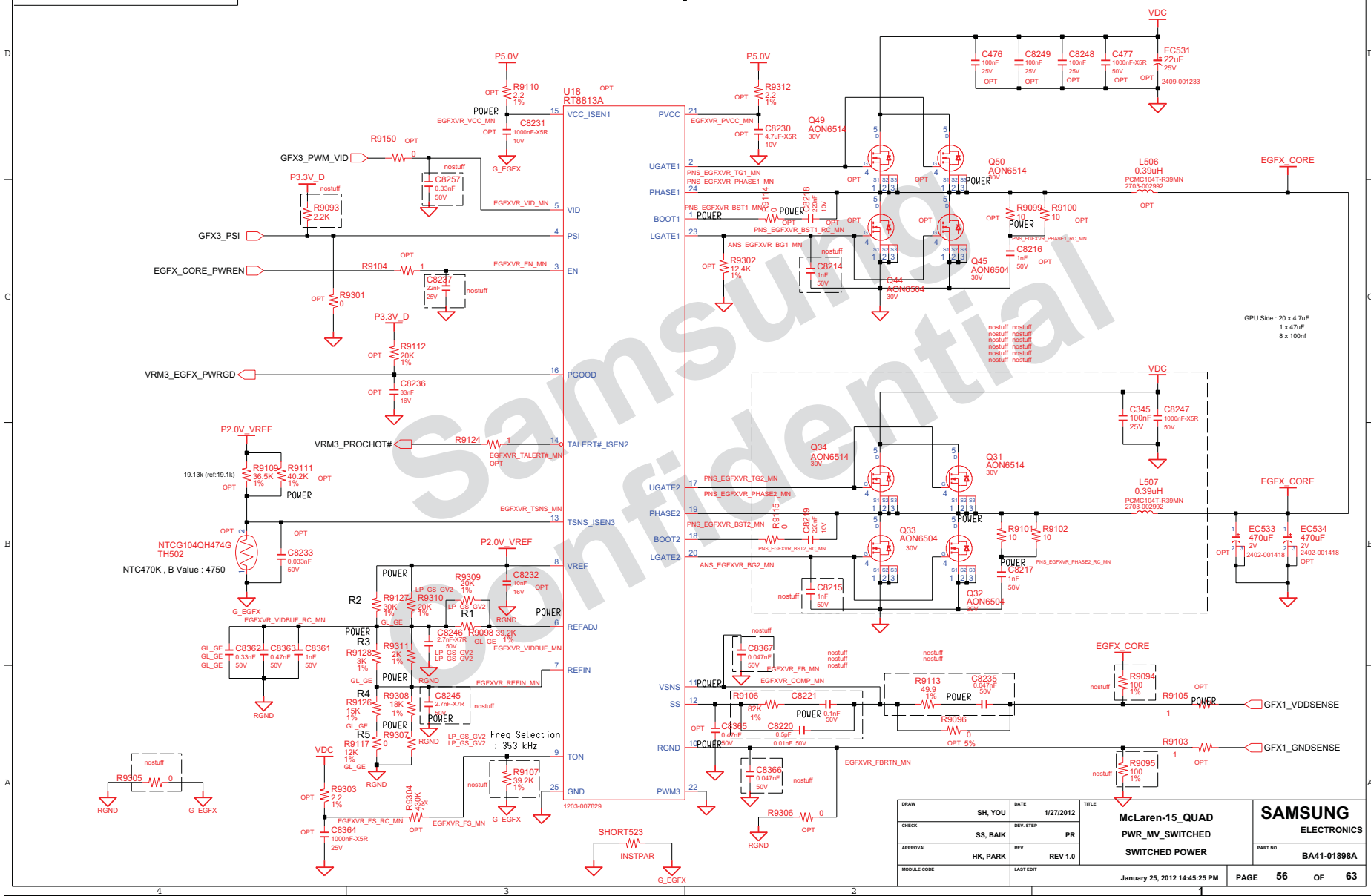
DRAW	RG Yang	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		P1.05V	
APPROVAL	BL Lee	REV	REV 1.0		VT386FCX	
MODULE CODE	undefined	LAST EDIT	July 31, 2012 13:21:52 PM			

PAGE 46 OF 53



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External Graphic Core Power

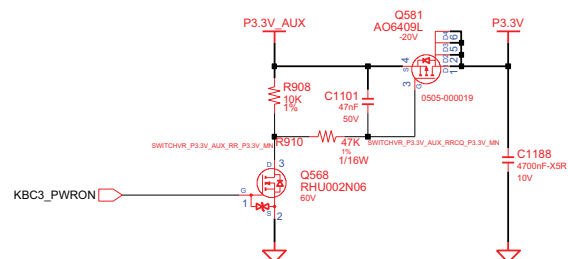


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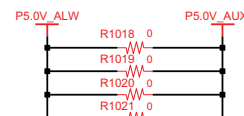
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Switched Power

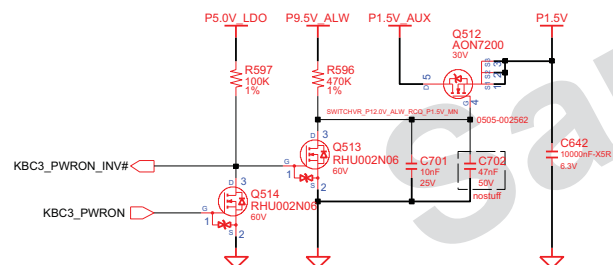
Switched Power On (P3.3V)



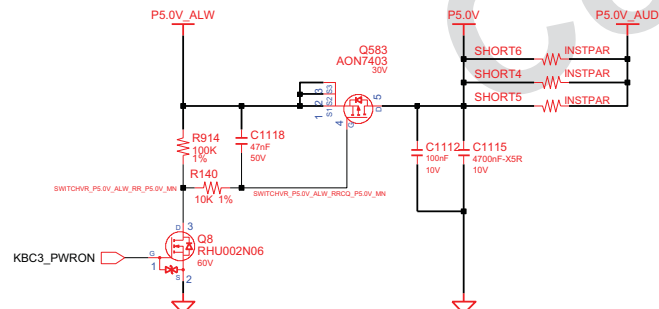
P5.0V_AUX



Switched Power On (P1.5V)



Switched Power On (P5.0V)



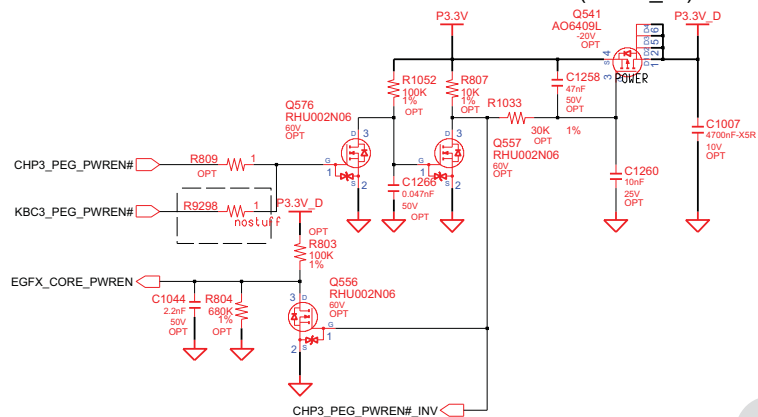
DRAW	RG Yang	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG
CHECK	RJ Zheng	DEV. STEP	PR	PWR_MV_SWITCHED	ELECTRONICS	
APPROVAL	BL Lee	REV	REV 1.0	SWITCHED POWER	PART NO.	BA41-*****A
MODULE CODE	LAST EDIT		July 31, 2012 13:21:52 PM		PAGE	49 OF 53

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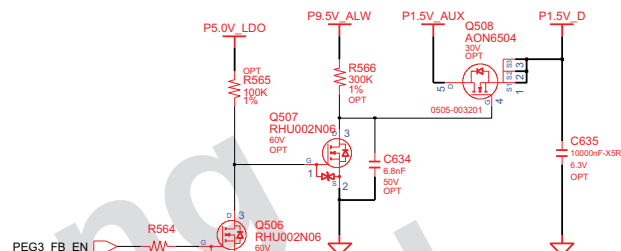
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Switched Power 2

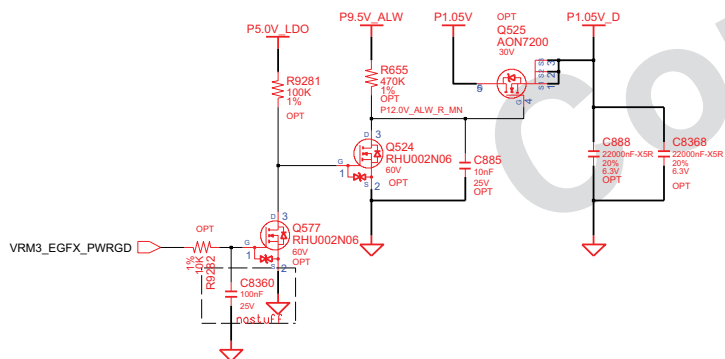
Discrete Switched Power (P3.3V_D)



Discrete Switched Power (P1.5V_D : MAX 5.3A)



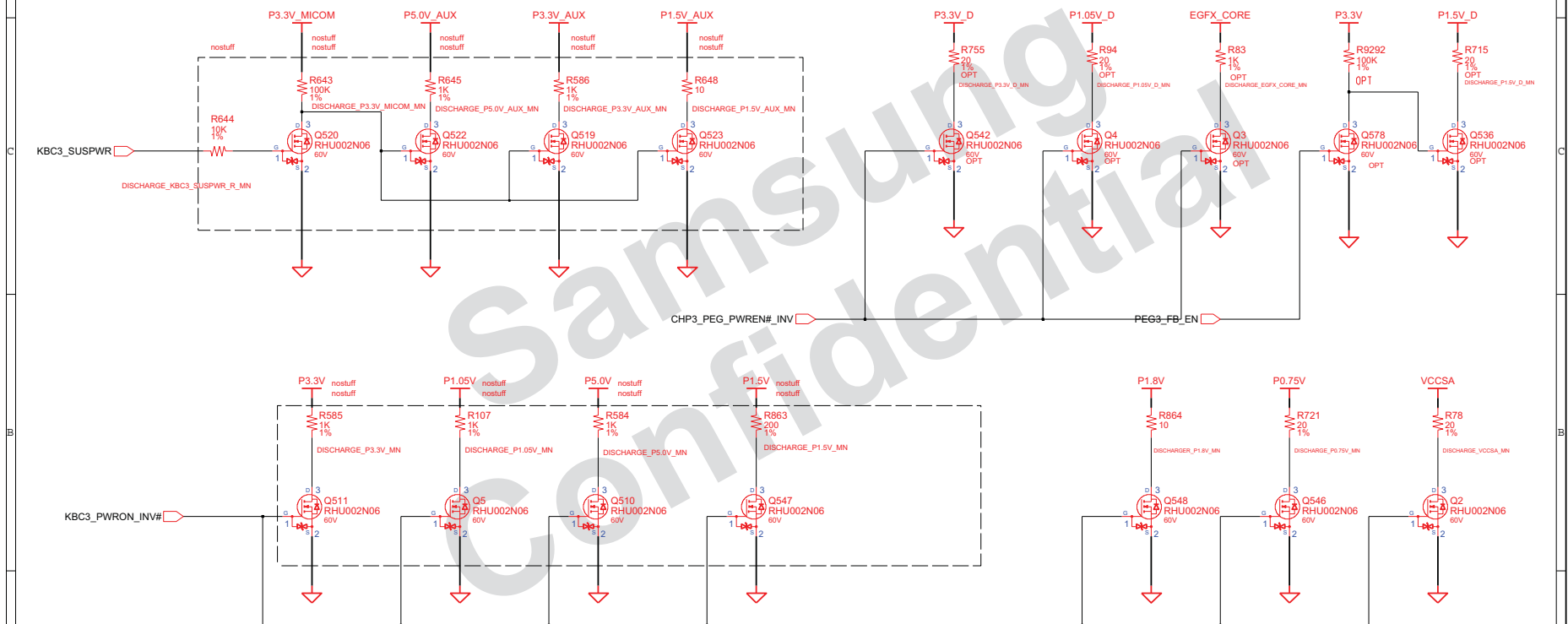
Discrete Switched Power (P1.05V_D)



DRAW	RG Yang	DATE	09/29/2012	TITLE Ramos-14/15 Switched PWR 2 Switched PWR 2	SAMSUNG ELECTRONICS	
CHECK	RJ Zheng	DEV. STEP	PR			
APPROVAL	BL Lee	REV	REV 1.0			
MODULE CODE		LAST EDIT				
July 31, 2012 13:21:52 PM					PART NO.	BA41-*****A
					PAGE	50 OF 53

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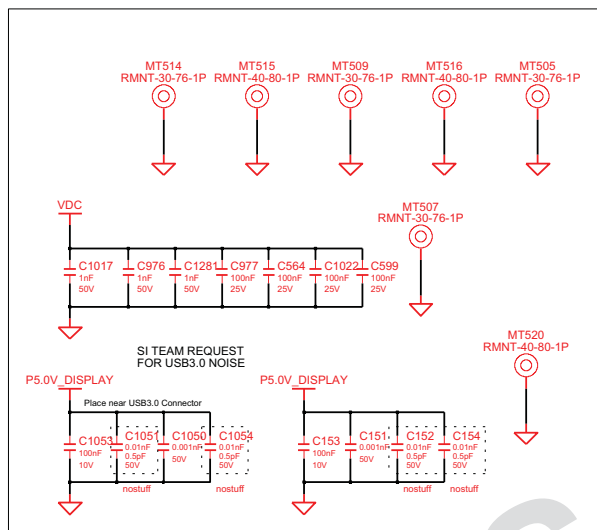
POWER DISCHARGER



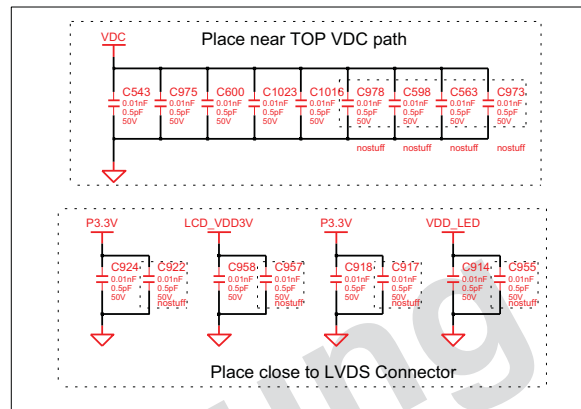
DRAW	RG Yang	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	REV. STEP	PR	PWR_MV_DISCHARGER		
APPROVAL	BL Lee	REV	REV 1.0	DISCHARGING LOGIC		PART NO.
MODULE CODE	undefined	LAST EDIT	July 31, 2012 13:21:52 PM			BA41-*****A
				PAGE	51	OF 53

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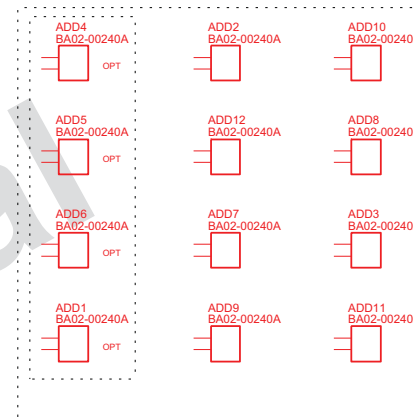
Mainboard Mount ((40-80)X2EA, (30-76)X5EA))



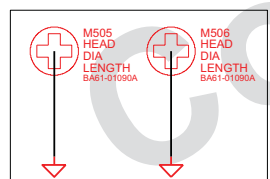
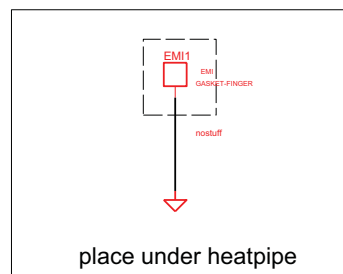
WLAN Performance issue



Corner Fill for CPU, PCH, GPU

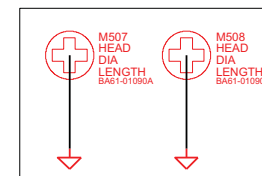


WLAN Performance issue



PCH mount

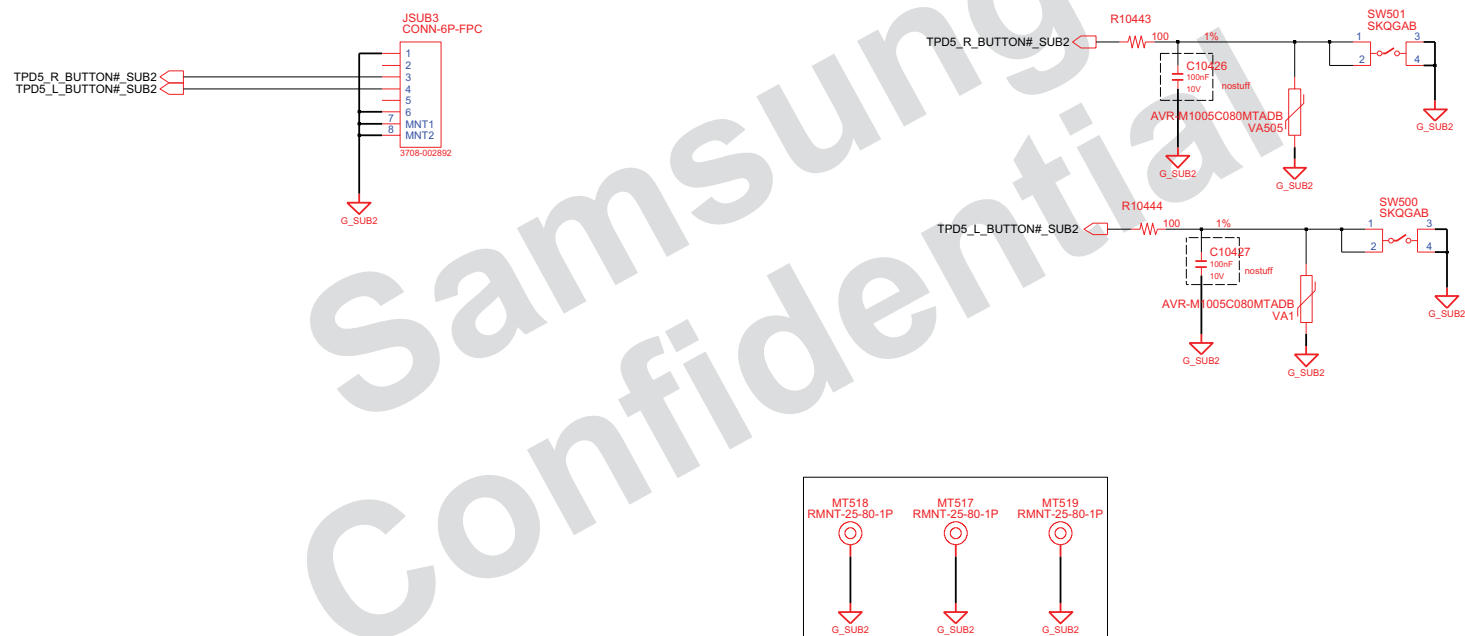
Memory Shield PEM




DESIGN	RG Yang	DATE	09/29/2012	TITLE	Ramos-14/15	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		MOUNT HOLE	
APPROVAL	BL Lee	REV	REV 1.0		MOUNT HOLE	
MODULE CODE		LAST EDIT				
				July 31, 2012 13:21:52 PM	PAGE	52 OF 53

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TP SUB BOARD



DRAWN	RG Yang	DATE	09/29/2012	Ramos-14/15 SUB2 TOUCHPAD & LED	
CHECKED	RJ Zheng	REV. STEP	PR		
APPROVAL	BL Lee	REV	REV 1.0		
MODULE CODE	LAST EDIT				
				July 31, 2012 13:21:52 PM	PAGE 53 OF 53